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Moore's Law And Linear Regression Based Prediction of Number of Transistors that Can Be Fitted on A Microprocessor In The Future

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Abstract— **Moore's law is the observation that the number of transistors in a dense integrated circuit (IC) doubles about every two years. Moore's law is an observation and projection of a historical trend. Rather than a law of physics, it is an empirical relationship linked to gains from experience in production. The observation is named after Gordon Moore, the co-founder of Fairchild Semiconductor and Intel (and former CEO of the latter), who in 1965 posited a doubling every year in the number of components per integrated circuit, and projected this rate of growth would continue for at least another decade. In 1975, looking forward to the next decade, he revised the forecast to doubling every two years, a compound annual growth rate (CAGR) of 41%. While Moore did not use empirical evidence in forecasting that the historical trend would continue, his prediction held since 1975 and has since become known as a "law."Moore's prediction has been used in the semiconductor industry to guide long-term planning and to set targets for research and development, thus functioning to some extent as a self-fulfilling prophecy. Advancements in digital electronics, such as the reduction in quality-adjusted microprocessor prices, the increase in memory capacity (RAM and flash), the improvement of sensors, and even the number and size of pixels in digital cameras, are strongly linked to Moore's law. These step changes in digital electronics have been a driving force of technological and social change, productivity, and economic growth. Industry experts have not reached a consensus on exactly when Moore's law will cease to apply. Microprocessor architects report that semiconductor advancement has slowed industry-wide since around 2010, below the pace predicted by Moore's law. However, as of 2018, leading semiconductor manufacturers have developed IC fabrication processes in mass production which are claimed to keep pace with Moore's law. In this study, the author studies Moore's Law in detail and uses it to predict using Linear Regression, the number of Transistors that can be fitted in an Integrated Circuit by 2050.**

***Index Terms*—Moore's Law. Linear Regression**

I. INTRODUCTION

Moore's Law

Moore's law is the observation that the number of transistors in a dense integrated circuit (IC) at optimal price/perfomance doubles about every two years. Moore's law is an observation and projection of a historical trend. Rather than a law of physics, it is an empirical relationship linked to gains from experience in production.

The observation is named after Gordon Moore, the co-founder of Fairchild Semiconductor and Intel (and former CEO of the latter), who in 1965 posited a doubling every year in the number of components per integrated circuit, and projected this rate of growth would continue for at least another decade. In 1975, looking forward to the next decade, he revised the forecast to doubling every two years, a compound annual growth rate (CAGR) of 41%. While Moore did not use empirical evidence in forecasting that the historical trend would continue, his prediction held since 1975 and has since become known as a "law."

Moore's prediction has been used in the semiconductor industry to guide long-term planning and to set targets for research and development, thus functioning to some extent as a self-fulfilling prophecy. Advancements in digital electronics, such as the reduction in quality-adjusted microprocessor prices, the increase in memory capacity (RAM and flash), the improvement of sensors, and even the number and size of pixels in digital cameras, are strongly linked to Moore's law. These step changes in digital electronics have been a driving force of technological and social change, productivity, and economic growth.

Industry experts have not reached a consensus on exactly when Moore's law will cease to apply. Microprocessor architects report that semiconductor advancement has slowed industry-wide since around 2010, below the pace predicted by Moore's law. However, as of 2018, leading semiconductor manufacturers have developed IC fabrication processes in mass production which are claimed to keep pace with Moore's law.

In 1959, Douglas Engelbart discussed the projected downscaling of integrated circuit (IC) size in the article "Microelectronics, and the Art of Similitude". Engelbart presented his ideas at the 1960 International Solid-State Circuits Conference, where Moore was present in the audience.

That same year, Mohamed Atalla and Dawon Kahng invented the MOSFET (metal–oxide–semiconductor field-effect transistor),

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also known as the MOS transistor, at Bell Labs. The MOSFET was the first truly compact transistor that could be miniaturized and mass-produced for a wide range of uses, with its high scalability and low power consumption resulting in a higher transistor density and making it possible to build high-density IC chips. In the early 1960s, Gordon E. Moore recognized that the ideal electrical and scaling characteristics of MOSFET devices would lead to rapidly increasing integration levels and unparalleled growth in electronic applications.

In 1965, Gordon Moore, who at the time was working as the director of research and development at Fairchild Semiconductor, was asked to contribute to the thirty-fifth anniversary issue of *Electronics* magazine with a prediction on the future of the semiconductor components industry over the next ten years. His response was a brief article entitled "Cramming more components onto integrated circuits".[1][11][b] Within his editorial, he speculated that by 1975 it would be possible to contain as many as 65,000 components on a single quarter-square-inch semiconductor.

The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years.

Moore posited a log-linear relationship between device complexity (higher circuit density at reduced cost) and time. In a 2015 interview, Moore noted of the 1965 article: "...I just did a wild extrapolation saying it's going to continue to double every year for the next 10 years."

In 1974, Robert H. Dennard at IBM recognized the rapid MOSFET scaling technology and formulated what became known as Dennard scaling, which describes that as MOS transistors get smaller, their power density stays constant such that the power use remains in proportion with area. MOSFET scaling and miniaturization have been the key driving forces behind Moore's law. Evidence from the semiconductor industry shows that this inverse relationship between power density and areal density broke down in the mid-2000s.

At the 1975 IEEE International Electron Devices Meeting, Moore revised his forecast rate, predicting semiconductor complexity would continue to double annually until about 1980, after which it would decrease to a rate of doubling approximately every two years. He outlined several contributing factors for this exponential behavior:

- The advent of metal–oxide–semiconductor (MOS) technology
- The exponential rate of increase in die sizes, coupled with a decrease in defective densities, with the result that semiconductor manufacturers could work with larger areas without losing reduction yields
- Finer minimum dimensions
- What Moore called "circuit and device cleverness"

Shortly after 1975, Caltech professor Carver Mead popularized the term "Moore's law". Moore's law eventually came to be widely accepted as a goal for the semiconductor industry, and it was cited by competitive semiconductor manufacturers as they strove to increase processing power. Moore viewed his eponymous law as surprising and optimistic: "Moore's law is a violation of Murphy's law. Everything gets better and better." The observation was even seen as a self-fulfilling prophecy.

The doubling period is often misquoted as 18 months because of a prediction by Moore's colleague, Intel executive David House. In 1975, House noted that Moore's revised law of doubling transistor count every 2 years in turn implied that computer chip performance would roughly double every 18 months (with no increase in power consumption). Moore's law is closely related to MOSFET scaling, as the rapid scaling and miniaturization of MOSFETs is the key driving force behind Moore's law. Mathematically, Moore's Law predicted that transistor count would double every 2 years due to shrinking transistor dimensions and other improvements. As a consequence of shrinking dimensions, Dennard scaling predicted that power consumption per unit area would remain constant. Combining these effects, David House deduced that computer chip performance would roughly double every 18 months. Also due to Dennard scaling, this increased performance would not be accompanied by increased power, i.e., the energy-efficiency of silicon-based computer chips roughly doubles every 18 months. Dennard scaling ended in the 2000s. Koomey later showed that a similar rate of efficiency improvement predated silicon chips and Moore's Law, for technologies such as vacuum tubes.

Microprocessor architects report that since around 2010, semiconductor advancement has slowed industry-wide below the pace predicted by Moore's law. Brian Krzanich, the former CEO of Intel, cited Moore's 1975 revision as a precedent for the current deceleration, which results from technical challenges and is "a natural part of the history of Moore's law". The rate of improvement in physical dimensions known as Dennard scaling also ended in the mid-2000s. As a result, much of the semiconductor industry has shifted its focus to the needs of major computing applications rather than semiconductor scaling. Nevertheless, leading semiconductor manufacturers TSMC and Samsung Electronics have claimed to keep pace with Moore's law with 10 nm and 7 nm nodes in mass production and 5 nm nodes in risk production

Moore's Second Law

As the cost of computer power to the consumer falls, the cost for producers to fulfill Moore's law follows an opposite trend: R&D, manufacturing, and test costs have increased steadily with each new generation of chips. Rising manufacturing costs are an important consideration for the sustaining of Moore's law. This had led to the formulation of Moore's second law, also called Rock's law, which is that the capital cost of a semiconductor fab also increases exponentially over time.

Consequences

Digital electronics have contributed to world economic growth in the late twentieth and early twenty-first centuries. The primary driving force of economic growth is the growth of productivity, and Moore's law factors into productivity. Moore (1995) expected that "the rate of technological progress is going to be controlled from financial realities". The reverse could and did occur around the late-1990s, however, with economists reporting that "Productivity growth is the key economic indicator of innovation." Moore's law describes a driving force of technological and social change, productivity, and economic growth.

An acceleration in the rate of semiconductor progress contributed to a surge in U.S. productivity growth, which reached 3.4% per year in

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1997–2004, outpacing the 1.6% per year during both 1972–1996 and 2005–2013. As economist Richard G. Anderson notes, "Numerous studies have traced the cause of the productivity acceleration to technological innovations in the production of semiconductors that sharply reduced the prices of such components and of the products that contain them (as well as expanding the capabilities of such products)."

The primary negative implication of Moore's law is that obsolescence pushes society up against the Limits to Growth. As technologies continue to rapidly "improve", they render predecessor technologies obsolete. In situations in which security and survivability of hardware or data are paramount, or in which resources are limited, rapid obsolescence often poses obstacles to smooth or continued operations.

Because of the intensive resource footprint and toxic materials used in the production of computers, obsolescence leads to serious harmful environmental impacts. Americans throw out 400,000 cell phones every day, but this high level of obsolescence appears to companies as an opportunity to generate regular sales of expensive new equipment, instead of retaining one device for a longer period of time, leading to industry using planned obsolescence as a profit centre.

An alternative source of improved performance is in microarchitecture techniques exploiting the growth of available transistor count. Out-of-order execution and on-chip caching and prefetching reduce the memory latency bottleneck at the expense of using more transistors and increasing the processor complexity. These increases are described empirically by Pollack's Rule, which states that performance increases due to microarchitecture techniques approximate the square root of the complexity (number of transistors or the area) of a processor.

For years, processor makers delivered increases in clock rates and instruction-level parallelism, so that single-threaded code executed faster on newer processors with no modification. Now, to manage CPU power dissipation, processor makers favor multi-core chip designs, and software has to be written in a multi-threaded manner to take full advantage of the hardware. Many multi-threaded development paradigms introduce overhead, and will not see a linear increase in speed vs number of processors. This is particularly true while accessing shared or dependent resources, due to lock contention. This effect becomes more noticeable as the number of processors increases. There are cases where a roughly 45% increase in processor transistors has translated to roughly 10–20% increase in processing power.

On the other hand, manufacturers are adding specialized processing units to deal with features such as graphics, video, and cryptography. For one example, Intel's Parallel JavaScript extension not only adds support for multiple cores, but also for the other non-general processing features of their chips, as part of the migration in client side scripting toward HTML5.

Moore's law has affected the performance of other technologies significantly: Michael S. Malone wrote of a Moore's War following the apparent success of shock and awe in the early days of the Iraq War. Progress in the development of guided weapons depends on electronic technology. Improvements in circuit density and low-power operation associated with Moore's law also have contributed to the development of technologies including mobile telephones and 3-D printing.

Forecasts

In April 2005, Gordon Moore stated in an interview that the projection cannot be sustained indefinitely: "It can't continue forever. The nature of exponentials is that you push them out and eventually disaster happens." He also noted that transistors eventually would reach the limits of miniaturization at atomic levels:

In terms of size [of transistors] you can see that we're approaching the size of atoms which is a fundamental barrier, but it'll be two or three generations before we get that far—but that's as far out as we've ever been able to see. We have another 10 to 20 years before we reach a fundamental limit. By then they'll be able to make bigger chips and have transistor budgets in the billions.

In 2016 the International Technology Roadmap for Semiconductors, after using Moore's Law to drive the industry since 1998, produced its final roadmap. It no longer centered its research and development plan on Moore's law. Instead, it outlined what might be called the More than Moore strategy in which the needs of applications drive chip development, rather than a focus on semiconductor scaling. Application drivers range from smartphones to AI to data centers.

IEEE began a road-mapping initiative in 2016, Rebooting Computing, named the International Roadmap for Devices and Systems (IRDS).

Most forecasters, including Gordon Moore, expect Moore's law will end by around 2025. Although Moore's Law will reach a physical limitation, many forecasters are optimistic about the continuation of technological progress in a variety of other areas, including new chip architectures, quantum computing, and AI and machine learning.

Major Enabling Factors

Numerous innovations by scientists and engineers have sustained Moore's law since the beginning of the IC era. Some of the key innovations are listed below, as examples of breakthroughs that have advanced integrated circuit and semiconductor device fabrication technology, allowing transistor counts to grow by more than seven orders of magnitude in less than five decades.

- Integrated circuit – The *raison d'être* for Moore's law. The germanium hybrid IC was invented by Jack Kilby at Texas Instruments in 1958, followed by the invention of the silicon monolithic IC chip by Robert Noyce at Fairchild Semiconductor in 1959.
- MOSFET – Invented at Bell Labs in 1959, it was the first transistor that could be miniaturized and mass produced, due to its high scalability.
    - CMOS (complementary metal-oxide-semiconductor) – The CMOS process was invented by Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor in 1963.
    - Dynamic random-access memory (DRAM) – Bipolar DRAM was developed by Toshiba in

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1965, and then MOS DRAM was independently developed by Robert H. Dennard at IBM in 1967. MOS DRAM made it possible to fabricate single-transistor memory cells on IC chips.

- Chemically-amplified photoresist – Invented by Hiroshi Ito, C. Grant Willson and J. M. J. Fréchet at IBM *circa* 1980, which was 5-10 times more sensitive to ultraviolet light. IBM introduced chemically amplified photoresist for DRAM production in the mid-1980s.

- Deep UV excimer laser photolithography – Invented by Kanti Jain at IBM *circa* 1980. Prior to this, excimer lasers had been mainly used as research devices since their development in the 1970s. From a broader scientific perspective, the invention of excimer laser lithography has been highlighted as one of the major milestones in the 50-year history of the laser.

- Interconnect innovations – Interconnect innovations of the late 1990s, including chemical-mechanical polishing or chemical mechanical planarization (CMP), trench isolation, and copper interconnects—although not directly a factor in creating smaller transistors—have enabled improved wafer yield, additional layers of metal wires, closer spacing of devices, and lower electrical resistance.

Computer industry technology road maps predicted in 2001 that Moore's law would continue for several generations of semiconductor chips.

Recent Trends

One of the key challenges of engineering future nanoscale transistors is the design of gates. As device dimension shrinks, controlling the current flow in the thin channel becomes more difficult. Compared to FinFETs, which have gate dielectric on three sides of the channel, gate-all-around MOSFET (GAAFET) structure has even better gate control.

- A gate-all-around MOSFET was first demonstrated in 1988, by a Toshiba research team led by Fujio Masuoka, who demonstrated a vertical nanowire GAAFET which he called a "surrounding gate transistor" (SGT). Masuoka, best known as the inventor of flash memory, later left Toshiba and founded Unisantis Electronics in 2004 to research surrounding-gate technology along with Tohoku University.

- In 2006, a team of Korean researchers from the Korea Advanced Institute of Science and Technology (KAIST) and the National Nano Fab Center developed a 3 nm transistor, the world's smallest nanoelectronic device at time, based on FinFET technology.

- In 2010, researchers at the Tyndall National Institute in Cork, Ireland announced a junctionless transistor. A control gate wrapped around a silicon nanowire can control the passage of electrons without the use of junctions or doping. They claim these may be produced at 10-nanometer scale using existing fabrication techniques.

- In 2011, researchers at the University of Pittsburgh announced the development of a single-electron transistor, 1.5 nanometers in diameter, made out of oxide-based materials. Three "wires" converge on a central "island" that can house one or two electrons. Electrons tunnel from one wire to another through the island. Conditions on the third wire result in distinct conductive properties including the ability of the transistor to act as a solid state memory. Nanowire transistors could spur the creation of microscopic computers.

- In 2012, a research team at the University of New South Wales announced the development of the first working transistor consisting of a single atom placed precisely in a silicon crystal (not just picked from a large sample of random transistors). Moore's law predicted this milestone to be reached for ICs in the lab by 2020.

- In 2015, IBM demonstrated 7 nm node chips with silicon-germanium transistors produced using EUVL. The company believes this transistor density would be four times that of current 14 nm chips.

- Samsung and TSMC plan to manufacture 3 nm GAAFET nodes by 2021–2022. Note that node names, such as 3 nm, have no relation to the physical size of device elements (transistors).

- A Toshiba research team including T. Imoto, M. Matsui and C. Takubo developed a "System Block Module" wafer bonding process for manufacturing 3D IC packages in 2001. In April 2007, Toshiba introduced an eight-layer 3D IC, the 16 GB THGAM embedded NAND flash memory chip which was manufactured with eight stacked 2 GB NAND flash chips. In September 2007, Hynix introduced 24-layer 3D IC, a 16 GB flash memory chip that was manufactured with 24 stacked NAND flash chips using a wafer bonding process.

- V-NAND, also known as 3D NAND, allows flash memory cells to be stacked vertically using charge trap flash technology originally presented by John Szedon in 1967, significantly increasing the number of transistors on a flash memory chip. 3D NAND was first announced by Toshiba in 2007. V-NAND was first commercially manufactured by Samsung Electronics in 2013.

- In 2008, researchers at HP Labs announced a working memristor, a fourth basic passive circuit element whose existence only had been theorized previously. The memristor's unique properties permit the creation of smaller and better-performing electronic devices.

- In 2014, bioengineers at Stanford University developed a circuit modeled on the human brain. Sixteen "Neurocore" chips simulate one million neurons and billions of synaptic connections, claimed to be 9,000 times faster as well as more energy efficient than a typical PC.

- In 2015, Intel and Micron announced 3D XPoint, a non-volatile memory claimed to be significantly faster with similar density compared to NAND. Production scheduled to begin in 2016 was delayed until the second half of 2017.

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- In 2017, Samsung combined its V-NAND technology with eUFS 3D IC stacking to produce a 512 GB flash memory chip, with eight stacked 64-layer V-NAND dies. In 2019, Samsung produced a 1 TB flash chip with eight stacked 96-layer V-NAND dies, along with quad-level cell (QLC) technology (4-bit per transistor), equivalent to 2 trillion transistors, the highest transistor count of any IC chip.
- In 2020, Samsung Electronics plans to produce the 5 nm node, using FinFET and EUV technology.
- In May 2021, IBM announces the creation of the first 2 nm computer chip, with supposedly parts being smaller than human DNA.

Microprocessor architects report that semiconductor advancement has slowed industry-wide since around 2010, below the pace predicted by Moore's law. Brian Krzanich, the former CEO of Intel, announced, "Our cadence today is closer to two and a half years than two." Intel stated in 2015 that improvements in MOSFET devices have slowed, starting at the 22 nm feature width around 2012, and continuing at 14 nm.

The physical limits to transistor scaling have been reached due to source-to-drain leakage, limited gate metals and limited options for channel material. Other approaches are being investigated, which do not rely on physical scaling. These include the spin state of electron spintronics, tunnel junctions, and advanced confinement of channel materials via nano-wire geometry. Spin-based logic and memory options are being developed actively in labs.

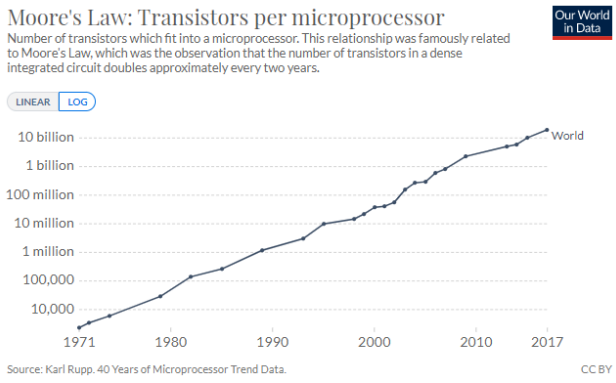

Fig 1 - Moore's Law: Transistors Per Microprocessor (Log Plot)

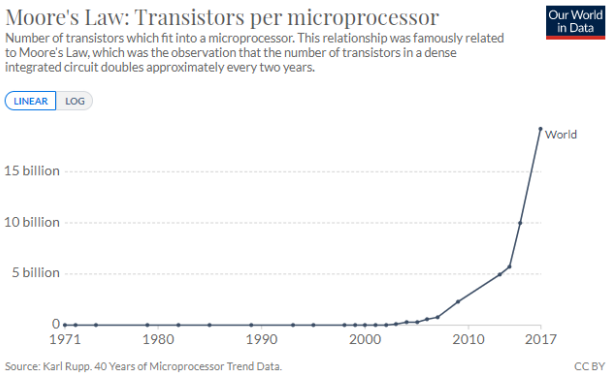

Fig 2 - Moore's Law: Transistors Per Microprocessor (Linear Plot)

II. RESULTS

Data

Year=(1971, 1972, 1974, 1980, 1982, 1985, 1989, 1993, 1995, 1998, 1999, 2000, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2009, 2013, 2014, 2015, 2017)

TransistorsPerMicroprocessor=(2308, 3555, 6098, 29164, 135773, 273842, 1210000, 3110000, 9650000, 15260000, 21670000, 37180000, 42550000, 55730000, 151250000, 273840000, 305050000, 582940000, 805840000, 2310000000, 5000000000, 5700000000, 10000000000, 19200000000)

For better Linear Regression Results, we take Log of the Transistors Per Microprocessor.

Table 1 – Data Table

Year	*TransistorsPer Microprocessor*	*Log(TransistorsPer Microprocessor)*
1971	2308	3.363235804
1972	3555	3.550839605
1974	6098	3.78518742
1980	29164	4.46484709
1982	135773	5.132813414
1985	273842	5.437500058
1989	1210000	6.08278537
1993	3110000	6.492760389
1995	9650000	6.984527313
1998	15260000	7.183554534
1999	21670000	7.335858911
2000	37180000	7.570309385
2001	42550000	7.628899564
2002	55730000	7.746089043
2003	1.51E+08	8.179695383
2004	2.74E+08	8.437496886
2005	3.05E+08	8.484371029
2006	5.83E+08	8.765623857
2007	8.06E+08	8.906248821
2009	2.31E+09	9.36361198

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2013	5E+09	9.698970004
2014	5.7E+09	9.755874856
2015	1E+10	10
2017	1.92E+10	10.28330123

R Program for Finding the Linear Regression Equation And Correlation Coefficient

```
rm(list=ls())

Year=c(1971, 1972, 1974, 1980, 1982, 1985, 1989,
1993, 1995, 1998, 1999, 2000, 2001, 2002, 2003,
2004, 2005, 2006, 2007, 2009, 2013, 2014, 2015,
2017)

TransistorsPerMicroprocessor=c(3.363235804,
3.550839605, 3.78518742, 4.46484709,
5.132813414, 5.437500058, 6.08278537,
6.492760389, 6.984527313, 7.183554534,
7.335858911, 7.570309385, 7.628899564,
7.746089043, 8.179695383, 8.437496886,
8.484371029, 8.765623857, 8.906248821,
9.36361198, 9.698970004, 9.755874856, 10,
10.28330123)

plot(Year, TransistorsPerMicroprocessor,
xlab="Year",
ylab="TransistorsPerMicroprocessor",
main="Year Vs TransistorsPerMicroprocessor")
lm1 <- lm(TransistorsPerMicroprocessor~Year)
plot(lm1)
summary(lm1)
cor(Year,TransistorsPerMicroprocessor)
```

R Program Results

```
R version 4.0.1 (2020-06-06) -- "See Things N
ow"
Copyright (C) 2020 The R Foundation for Stati
stical Computing
Platform: x86_64-w64-mingw32/x64 (64-bit)

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butors.
Type 'contributors()' for more information an
d
'citation()' on how to cite R or R packages i
n publications.

Type 'demo()' for some demos, 'help()' for on
-line help, or
'help.start()' for an HTML browser interface
to help.
Type 'q()' to quit R.

[Workspace loaded from ~/.RData]

> rm(list=ls())
> Year=c(1971, 1972, 1974, 1980, 1982, 1985,
1989, 1993, 1995, 1998, 1999, 2000, 2001, 200
2, 2003, 2004, 2005, 2006, 2007,
+        2009, 2013, 2014, 2015, 2017)
> TransistorsPerMicroprocessor=c(3.363235804,
 3.550839605, 3.78518742, 4.46484709, 5.13281
3414, 5.437500058, 6.08278537,
+                                6.492760389,
6.984527313, 7.183554534, 7.335858911, 7.5703
09385, 7.628899564, 7.746089043, 8.179695383,
8.437496886,
+                                8.484371029,
8.765623857, 8.906248821, 9.36361198, 9.69897
0004, 9.755874856, 10, 10.28330123)
> plot(Year, TransistorsPerMicroprocessor,
+      xlab="Year",
+      ylab="TransistorsPerMicroprocessor ",
+      main="Year Vs TransistorsPerMicroproce
ssor")
> lm1 <- lm(TransistorsPerMicroprocessor~Year
)
> plot(lm1)
Hit <Return> to see next plot: summary(lm1)
Hit <Return> to see next plot: cor(Year,Trans
istorsPerMicroprocessor)
Hit <Return> to see next plot:
Hit <Return> to see next plot:
>
> plot(lm1)
Hit <Return> to see next plot:
Hit <Return> to see next plot:
Hit <Return> to see next plot:
Hit <Return> to see next plot:
>
> summary(lm1)

Call:
lm(formula = TransistorsPerMicroprocessor ~ Y
ear)

Residuals:
     Min       1Q   Median       3Q      Max
-0.25142 -0.12732  0.03091  0.08066  0.30346

Coefficients:
             Estimate Std. Error t value Pr(
>|t|)
(Intercept) -2.959e+02  4.500e+00  -65.76   <
2e-16 ***
Year         1.518e-01  2.253e-03   67.38   <
2e-16 ***
---
Signif. codes:  0 ‘***’ 0.001 ‘**’ 0.01 ‘*’ 0
.05 ‘.’ 0.1 ‘ ’ 1

Residual standard error: 0.1489 on 22 degrees
of freedom
Multiple R-squared:  0.9952,      Adjusted R-
squared:  0.995
F-statistic:  4540 on 1 and 22 DF,  p-value:
< 2.2e-16

> cor(Year,TransistorsPerMicroprocessor)
[1] 0.9975857
>
```

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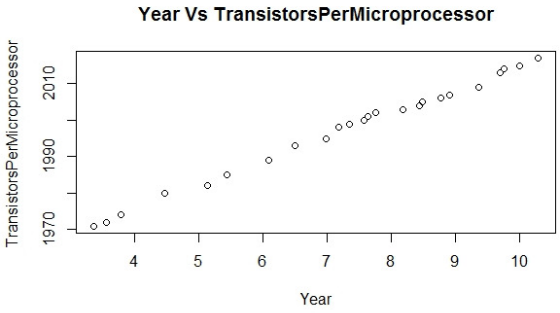

Fig 3 - Year Vs TransistorsPerMicroProcessor

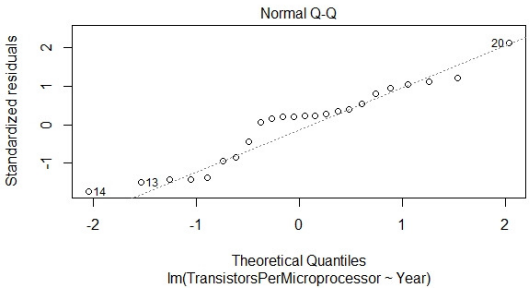

Fig 4 - Normal Q-Q Plot

A Q-Q plot is a scatterplot created by plotting two sets of quantiles against one another. If both sets of quantiles came from the same distribution, we should see the points forming a line that's roughly straight. Here's an example of a Normal Q-Q plot when both sets of quantiles truly come from Normal distributions.

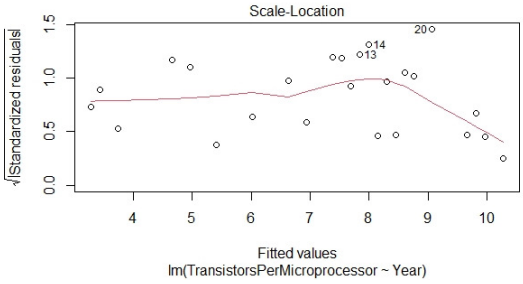

Fig 5 - Scale-Location Plot

The scale location plot helps us check a regression model for violations of linearity and homoskedasticity.

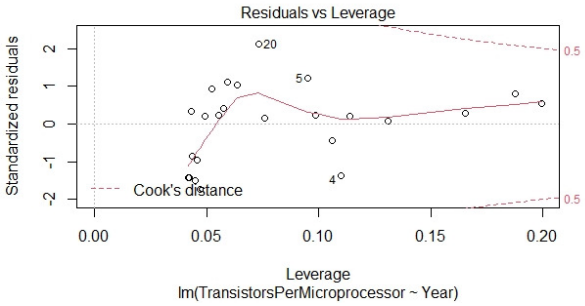

Fig 6 - Residuals Vs Leverage Plot

The Residuals vs. Leverage plots helps to identify influential data points on the model. outliers can be influential, though they don't necessarily have to it and some points within a normal range in your model could be very influential. Outliers: defined as an observation that has a large residual.

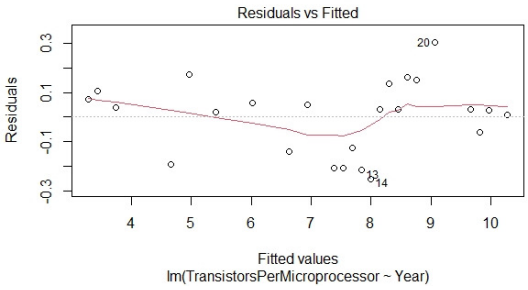

Fig 7 - Residuals Vs Fitted Plot

When conducting a residual analysis, a "residuals versus fits plot" is the most frequently created plot. It is a scatter plot of residuals on the y axis and fitted values (estimated responses) on the x axis. The plot is used to detect non-linearity, unequal error variances, and outliers.

Results: Linear Regression Equation & Correlation Coefficient

We have used R Programming Language to compute the Linear Regression Equation and Correlation Coefficient for the aforecomputed case:

The governing Linear Regression Equation is

$$y = mx + c$$

$$y = (1.518e-01)x - (2.959e+02)$$

That is $y = 0.1518x - 295.9$

where

x = Year

y = Log(Transistors Per Microprocessor)

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Table 2 –Linear Regression Based Predictions

Year	*Log(Predicted Transistors Per Microprocessor)*	*Predicted Transistors Per Microprocessor*
2020	10.736	54450265284
2021	10.8878	77232483446
2022	11.0396	1.09547E+11
2025	11.495	3.12608E+11
2030	12.254	1.79473E+12
2035	13.013	1.03039E+13
2040	13.772	5.91562E+13
2045	14.531	3.39625E+14
2050	15.29	1.94984E+15

III. CONCLUSIONS

1. The number of Transistors that can be fitted in a Microprocessor in the future years is computed from Linear Regression Based Prediction as follows:

Table 3 –Linear Regression Based Predictions

Year	*Log(Predicted Transistors Per Microprocessor)*	*Predicted Transistors Per Microprocessor*
2020	10.736	54450265284
2021	10.8878	77232483446
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2045	14.531	3.39625E+14
2050	15.29	1.94984E+15

2. The regression line is important as it makes the estimation of a dependent variable more accurate and it allows the estimation of a response variable for individuals with values of the carrier variable not included in the data.
3. The Residuals Vs Fitted graph looks good. It is used to used to detect non-linearity, unequal error variances, and outliers. From this graph we can note that there is not much non-linearity, there are not any outliers and there is no case of unequal error variances.
4. The Residuals Vs Leverage Plot also looks good. The Residuals vs. Leverage plots helps to identify influential data points on the model. From this graph we can note that there are not any points that significantly influence the model askewly.
5. The Scale-Location Plot also looks good. From this graph, we can note that there are not any violations of linearity and instances of homoscedasticity.
6. The Quantile-Quantile Plot also looks good. From this graph, we can note that the two sets of Quantiles of the two x and y variable distributions plotted against each other is quite linear and hence well explains the high coefficient of correlation between x and y.

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