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REALIZATION OF FIR FILTER BY USING LOW POWER ADDER WITH PASS TRANSISTOR LOGIC

[1]NANTHAKUMAR.K
[2]S.Jenifer Berlin , [3]M.Indhumathi, [4]S.Santhiya, [5]M.Mahalakshmi
[1]Assistant Professor, Department of ECE, M.P.Nachimuthu M.Jaganathan Engineering College, Erode.
Mail id : nanthakumarece5@gmail.com
2-5 Final Year, Department of ECE, M.P.Nachimuthu M.Jaganathan Engineering College, Erode.

ABSTRACT

The Finite Impulse Response (FIR) filter are a class of digital filter that have finite impulse response.The proposed adder was designed by Pass Transistor Logic(PTL).In FIR filter realization the existing adder was replaced by the proposed adder ,which reduces the power.VLSI designers often choose static CMOS logic style for low power applications. This logic style provides low power dissipation and is free from signal noise integrity issues. On the other hand designs based on Domino logic style yield highoccupy less area.In this paper CMOS full adder circuits are designed to reduce the power. Comparative analysis for the proposed design out performance is measured in terms of power, area. A new Pass transistor full adder circuit is implemented in this paper. The main idea is to introduce the design of based pass transistor full adders which acquires less area and transistor count. The result shows that the proposed full adder is an efficient full adder with least MOS transistor count that reduces the high power consumption and reduce the size.

INTRODUCTION

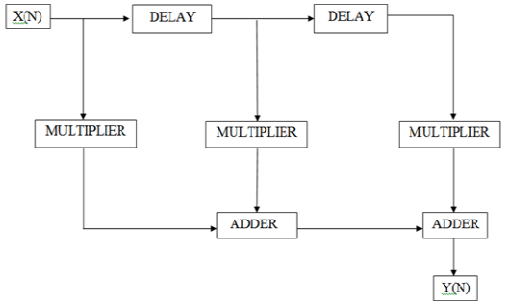

Fig. 1 Structure of FIR Filter

FIR filter realization have three main elements.

(i) Adder
(ii) Delay element
(iii) Multiplier

The Fig.1 shows that X(N) is the input signal.Y(N) is the output signal.Delay is single bit. So D-Flipflop is used here.The proposed low power adder using PTL is used here.Array multiplier is a digital combinational circuitused for multiplying two binary numbers by employing an array of full adders and halfadders. A filter whose response has finite duration, because it settles to zero in finite time. Non recursive since unlike IIR filters. Its construction generally uses Direct form and Cascade form. The impulse response of an Nth order discrete time FIR filter takes precisely N+1 samples before it then settles to zero. FIR filters are most popular kind of filters executed in software and these filters can be continuous time, analog or digital and

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discrete time. The filter design can be defined as, it is the process of choosing the length and coefficients of the filter.

EXISTING METHOD

STATIC CMOS LOGIC

Fig.2 shows that static CMOS logic, the output is connected to ground through an n-block and to VDD is through a dual p-block. Static logic circuits allow versatileimplementation of logic functions based on static or steady-state, behavior of simple CMOS structures.

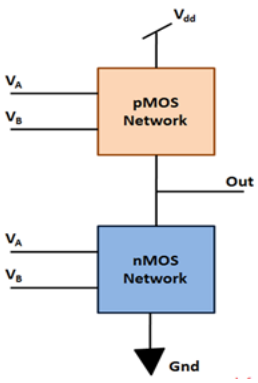

Fig. 2 Static CMOS logic

EXAMPLE

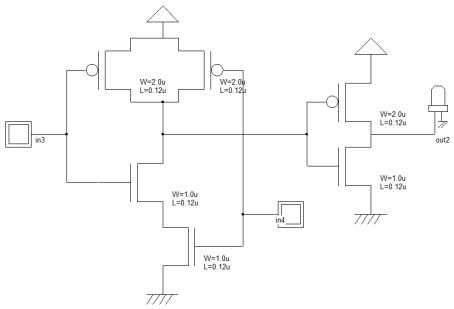

Fig. 3 2-Input AND Gate using Static CMOS Logic Style

DOMINO CMOS LOGIC

Fig. 4 shows that Domino logic is a CMOS based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors.It allows a rail to rail logic swing. It to develop for speed up circuits. Only non-inverting structures are possible because of the presenceof inverting buffer. Due to the absence of clock signal the circuits designed with static CMOS logic style have less switching activity.

Static CMOS logic is slower because it uses bulky PMOS transistors in its charging path.Domino logic circuits can implement only non-inverting logic.Domino logic style suffers from signal noise integrity issues.

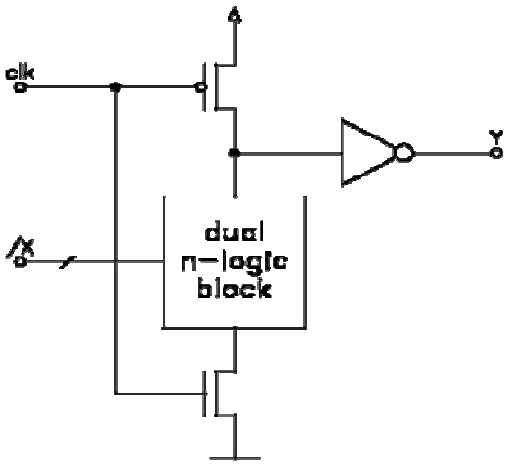

Fig. 4 Domino CMOS Logic

EXAMPLE

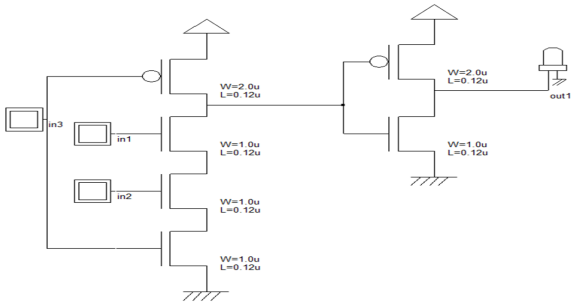

Fig. 5 2-Input AND Gate using Domino CMOS Logic Style

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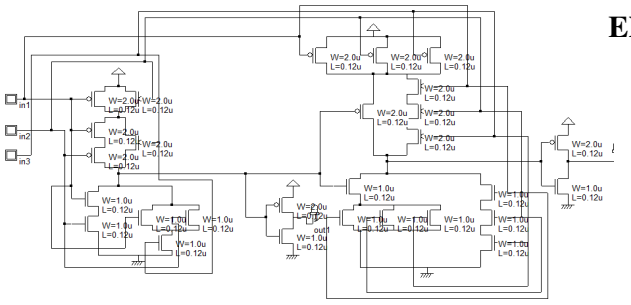

Fig.6 Schematic Diagram of Static CMOS Full Adder

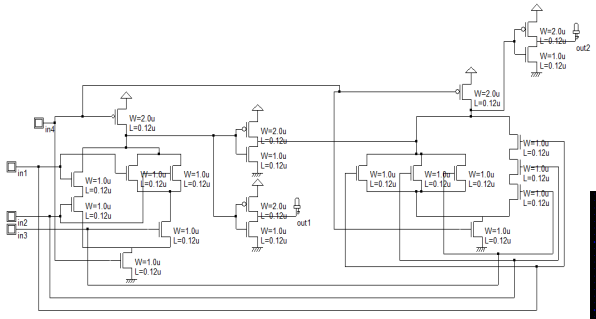

Fig.7 Schematic Diagram of Domino CMOS Full Adder

PROPOSED METHOD:

Fig. 8 shows that PTLdescribes several logic families used in the designof integrated circuits.It reduces the count of transistors used to make different logic gates,by eliminating redundant transistors. PTL uses a nMOS or pMOS transistor to transfer charge from input node to theoutput node,under the control of gate voltage.

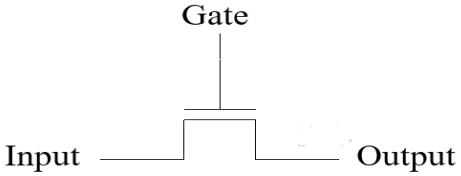

Fig. 8 Pass Transistor Logic

EXAMPLE

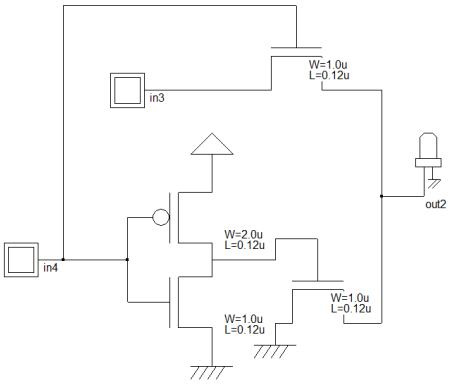

Fig.9 2-Input AND Gate using Pass Transistor Logic

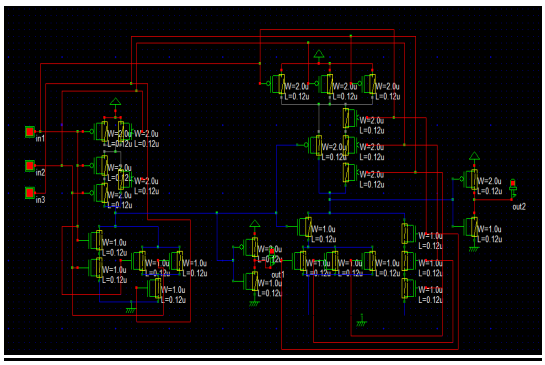

Fig.10 Schematic Diagram of Static CMOS Full Adder

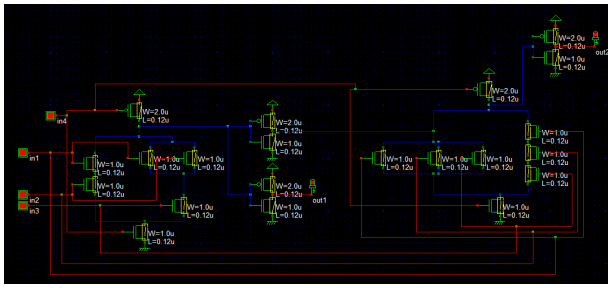

Fig.11 Schematic Diagram of Domino CMOS Full Adder

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OUTPUT FOR EXISTING METHOD

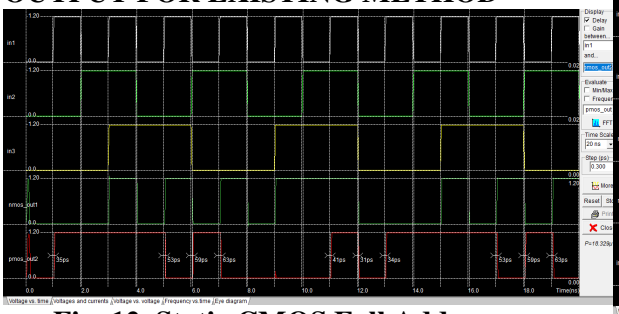

Fig. 12 Static CMOS Full Adder

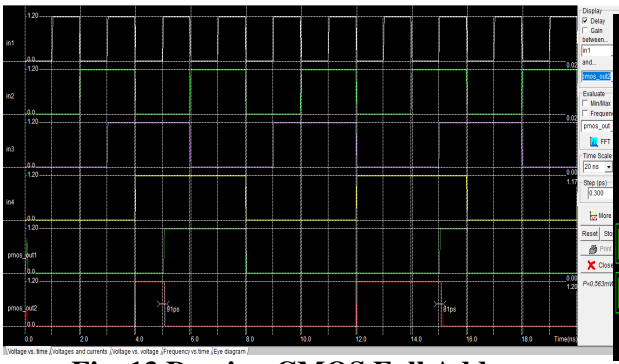

Fig. 13 Domino CMOS Full Adder

OUTPUT FOR PROPOSED METHOD

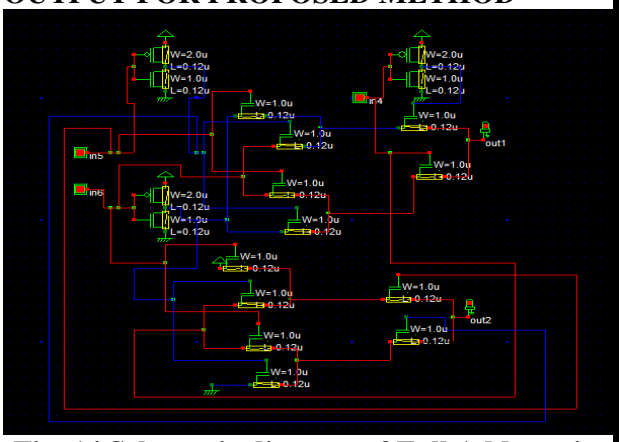

Fig. 14 Schematic diagram of Full Adder using Pass Transistor Logic

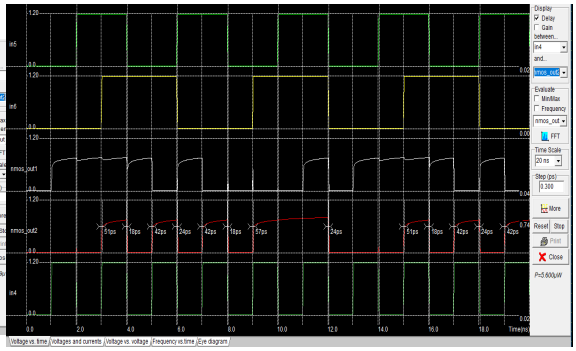

Fig.15 Full Adder using Pass Transistor Logic

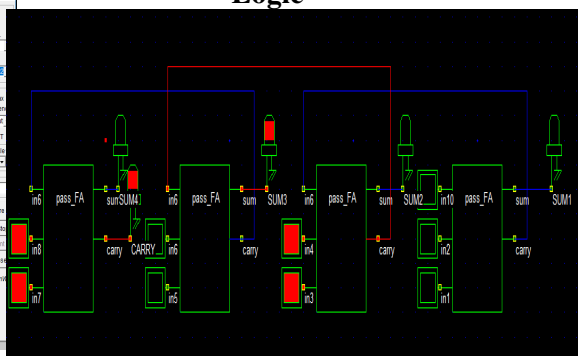

Fig. 16 Schematic diagram of 4-Bit Adder

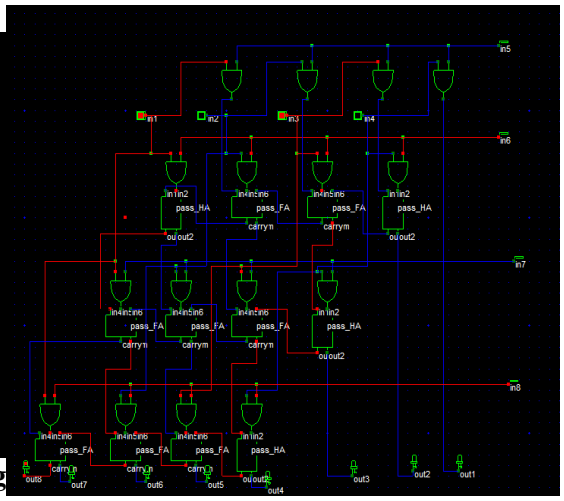

Fig. 17 Schematic Diagram of Array Multiplier

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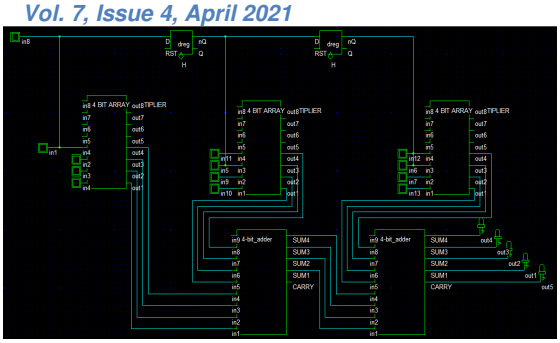

Fig. 18 Schematic Diagram of FIR Filter Realization

CONCLUSION

The 4-bit low power adder was designed by using PTL. Comparing the results of static and domino logic full adder. PTL power 55%,98% reduced. The major computational blocks of FIR filter are Adder, Multiplier and Delay elements in which designing a 4-bit adder circuit will make the FIR filter design low power consumption and area efficient. Then array multiplier was designed by using PTL based full adder. In FIR filter realization the proposed Adder and Multiplier was used which reduces the power.

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BIOGRAPHY

K.Nanthakumar completed his M.E VLSI in M.P.Nachimuthu M.Jaganathan Engineering College, Erode, Anna University, Chennai, Completed his B.E Electronics and Communication Engineering in M.P.Nachimuthu M.Jaganathan Engineering College, Erode. Now he is working as a Assistant Professor in ECE department in M.P.Nachimuthu M.Jaganathan Engineering College, Erode, India. He has 9 years of teaching experience. He has published more than 10 papers in various national and international journals. His area of interest is low power VLSI Design.

S.Jenifer Berlin has pursuing final B.E Electronics and Communication Engineering in

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M.P.Nachimuthu M.Jaganathan Engineering College, Erode, Anna University, Chennai, her area of interest is VLSI and Digital Signal Processing.

M.Indhumathi has pursuing final B.E Electronics and Communication Engineering in M.P.Nachimuthu M.Jaganathan Engineering College, Erode, Anna University, Chennai, her area of interest is Digital Signal Processing and Digital Electronics.

S.Santhiya has pursuing final B.E Electronics and Communication Engineering in M.P.Nachimuthu M.Jaganathan Engineering College, Erode, Anna University, Chennai, her area of interest is VLSI and Digital Image Processing.

M.Mahalakshmi has pursuing final B.E Electronics and Communication Engineering in M.P.Nachimuthu M.Jaganathan Engineering College, Erode, Anna University, Chennai her area of interest is VLSI and Communication Theory.