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IMPLEMENTATION OF HIGH PERFORMANCE FIR FILTER FOR FIXED AND RECONFIGURABLE APPLICATIONS

Emy P Thomas[1], S.Reeba Rex[2], Brinda.G[3]

[1] P.G Scholar, Dept. of ECE, Mar Ephraem College of Engineering & Technology
[2,3]Assistant Professor, Dept. of ECE, Mar Ephraem College of Engineering & Technology

Abstract- In this paper we derive a chance to realize the transpose form configuration of block FIR filter to provide area-delay efficiency of large and medium length FIR filters for fixed and reconfigurable applications. For fixed FIR filter has a generalized block formulation. From that we derive multiplier based architecture for proposed structure. The Proposed structure has lessADP and EPS than the existing direct form structure.

I. INTRODUCTION

Digital Signal Processing is the proper solution for all signal processing problems. The FIR filters are employed in filtering applications such as data and voice communications, speech processing, pulse shaping, software-defined radio etc,[1].Many of these applications require large order FIR filters to meet their frequency specifications. Adaptive filters are widely used in all of the above applications here we derived the DA formulation of BLMS algorithm [15].Distributed arithmetic based computation is popular for the efficient memory based implementation of FIR filters. The filter employed in mobile system must be realized to consume less power and operate at high speed. It will provide flexibility through reconfiguration [9].Distributed arithmetic can implement without multiplier unit where MAC unit can be replaced by a series of LUT access and Summations LUTs are the kind of logic that used in DRAM FPGAs [3]. Block Processing is used to provide high-throughput as well as improves the energy efficiency of the filter.

The MCM architecture is presented for the block implementation of fixed FIR filters. MCM methods used to reduce the total number of additions required for the realization of multiplications using common sub expression sharing. Sub expression sharing means given input is multiplied with a set of constants. MCM scheme is more effective because when a common operand is multiplied with multiple numbers of constants [2]. SDR is nothing but a radio communication system in which parts that have been regularly in hardware implementation are rather implemented through software on a personal computer or

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embedded system these will allow communication related securities[5][6].the FIR filters are always pipelined and that will support multiple constant multiplications. Thus the filters are pipelined that will provide high frequency at high sampling rate[12]. It is all well known that the Canonical Signed Digit representation can be used to reduce the complexity of FIR digital filter implementation Encoding the filter coefficients using the CSD representation reduces the number of partial products and thus saves silicon area and power consumption in computation hardware implementation thus the technique ispopular for fixed coefficient FIR filter implementation[8]. Christo Ananth et al. [4] proposed a system, this paper presents an effective field programmable gate array (FPGA)-based hardware implementation of a parallel key searching system for the brute-force attack on RC4 encryption. The design employs several novel key scheduling techniques to minimize the total number of cycles for each key search and uses on-chip memories of the FPGA to maximize the number of key searching units per chip. Based on the design, a total of 176 RC4 key searching units can be implemented in a single Xilinx XC2VP20-5 FPGA chip. Operating at a 47-MHz clock rate, the design can achieve a key searching speed of 1.07 x 107 keys per second. Breaking a 40-bit RC4 encryption only requires around 28.5 h. DAbased implementation requires LUTs to be implemented in RAM. The RAM based LUTs are costly so we use shared LUTs for the DA computation[10].DA is good way to trade combinational logic with memory for high performance computation [16][18].Recently VLSI DSP systems is used in video and image transmission and storage in order to achieve high speed and save the bandwidth. In this paper we explore the realization of transpose form configuration of FIR filter to provide area-delay efficiency of the proposed structure taking the advantage of MCM scheme and pipelining. The main contribution of this paper is as follows.

1. Computational analysis of the fir filter transpose form configuration.

2. multiplier based architecture for reconfigurable structure.

3 Take advantage of the MCM scheme.

4 low complexity design for the proposed structure.

II. COMPUTATIONAL ANALYSIS

FIR filter of length N has the output that has been computed using the relation

$$y(n) = \sum_{i=0}^{N-1} h(i) \cdot x(n-i). \quad (1)$$

The computation can be expressed by the recurrence relation

$$Y(z) = [z^{-1}(\cdots(z^{-1}(z^{-1}h(N-1)+h(N-2))+h(N-3)) \cdots + h(1))+h(0)]X(z). \quad (2)$$

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The data-flow graphs (DFG-1 and DFG-2) of transpose form FIR filter for filter length N=6, for a block of two successive outputs{y(n),y(n−1)} that are derived from. The product values and their accumulation paths in DFG-1 and DFG-2 of Fig. 1 are shown in data-flow tables (DFT-1 and DFT-2). The arrows in DFT-1 and DFT-2. 2 represent the accumulation path of the products. These redundant computations of DFG-1 and DFG-2 can be avoided using non overlapped sequence of input blocks, as shown in Figure. DFT-3 and DFT-4 of DFG-1 and DFG-2 for nonoverlapping input blocks are, respectively, shown in Figure. As shown in Figure DFT-3 and DFT-4 do not involve redundant computation. It is easy to find that the entries in the cells in DFT-3 and DFT-4 of Figure correspond to the output y(n), whereas the other entries of DFT-3 and DFT-4 correspond toy(n−1).The DFG of Figure needs to be transformed appropriately to obtain the computations according to DFT-3 and DFT-4. The DFG-3 can be retimed to obtain DFG-4.Using this output of transpose form FIR filter is y(n) we give the input value x(n) and filter coefficient h(n). For reconfigurable applications the filter coefficients are varying the proposed method is used to produce out with area delay efficiency when the filter coefficients are varying.

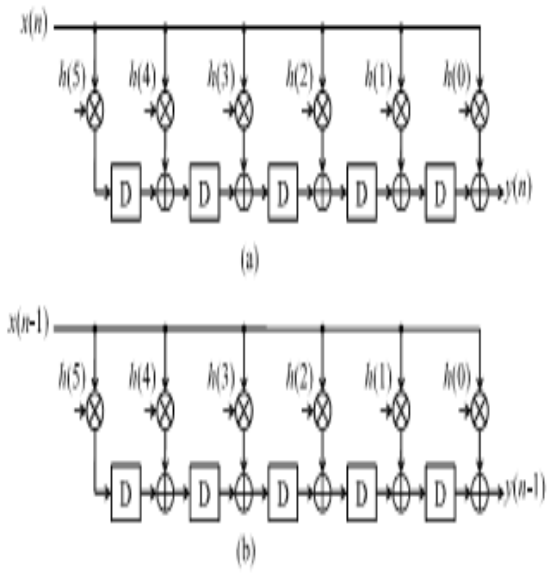

Fig.1 DFG of transpose form structure for N =6. (a) DFG-1 for output y(n). (b) DFG-2 for output y(n−1).

B. DFG Transformation

The computation of DFT-3 and DFT-4 can be realized by DFG-3 of non-overlapping blocks, as shown in Figure. We refer it to block transpose form type-I configuration of block FIR filter. The DFG-3 can be retimed to obtain the DFG-4 of Figure, which is referred to block transpose form type-II configuration. Note that both type-I and type-II configurations involve the same number of multipliers and adders, but type-II configuration involves nearly L times less delay elements than those of type-I configuration.

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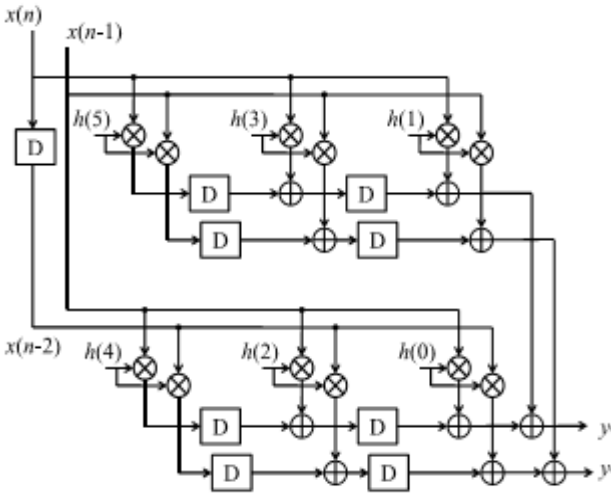

Fig.2 Merged DFG (DFG-3: transpose form type-I configuration for block FIR structure)

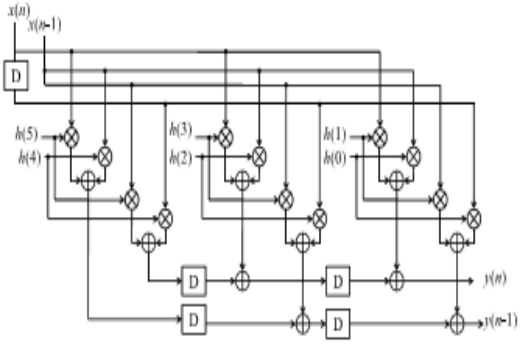

Fig.3 DFG-4 (retimed DFG-3) transpose form type-II configuration for block FIR structure.

In digital filter design , we describe frequency transformation in both analog and digital domains the FIR filter operate on present and past input values and are the simplest filters to design. The FIR filters implemented based on the distributed arithmetic method.

III. PROPOSED STRUCTURES

Most of the applications where the coefficients of all the FIR filters remain fixed, while in some other applications the coefficients are varied according to the run time. In a SDR they need separate FIR filters with different specification to extract desired narrow band signal from wide band. These type of filters must be implemented in a reconfigurable architecture that support wireless communication. Here we derive block FIR filter of fixed and reconfigurable application taking the advantage of MCM scheme.

IV. PROPOSED TECHNIQUE AND BLOCK DIAGRAM

From the fig.3 shows the proposed structure of block size L=4. It consist of one coefficient Selection Unit(CSU),one register unit (RU),one pipeline adder unit (PAU),M number of inner product unit(IPU).The CSU stores all the filter coefficient values to be used for reconfigurable applications. Here all the filters are pipelined. The RU receives x_k during the kth cycle and produces L rows of S^0_k in parallel. L rows of S^0_k are transmitted to MIPUs of the proposed structure. The MIPUs also receive M short-weight vectors from the CSU such that during the kth cycle, the (m+1)th IPU receives the weight vector cM−m−1 from

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the CSU and L rows of S^0_k form the RU. Register unit stores the input values and that can be given to the input product unit. where the multiplication of input values and coefficients from the coefficient storage unit.

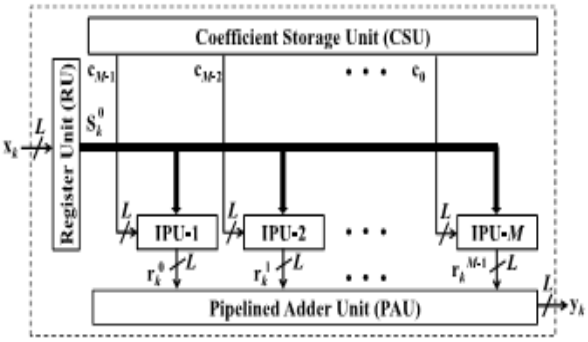

Fig.3: Proposed structure for block FIR filter

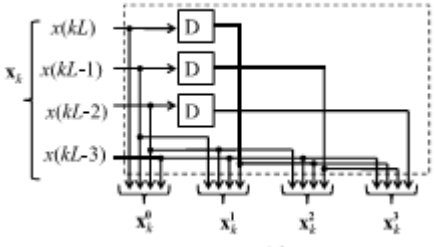

Fig.3.1 (Structure of (m+1)th IPU

The proposed structure receives a block of L inputs and L filter outputs, where the multiplication of coefficients and the input values after multiplication the values are given to the pipeline adder unit where the summation is carried outand the output is produced. In each cycle the proposed structure receives L inputs and produces block of L outputs. Where duration of each cycle is $T = T_M + T_A + T_{FA}\log_2 L$, T_M is the multiplier delay, T_A is the one adder delay, and T_{FA} is one full-adder delay.

V. SIMULATION RESULTS AND DISCUSSION

The following figure shows the simulation results.Fig.4 shows output of the block FIR filter .from the diagram we can learn that the area delay efficiency of the proposed system improves and has less area-delay product and less energy per sample.

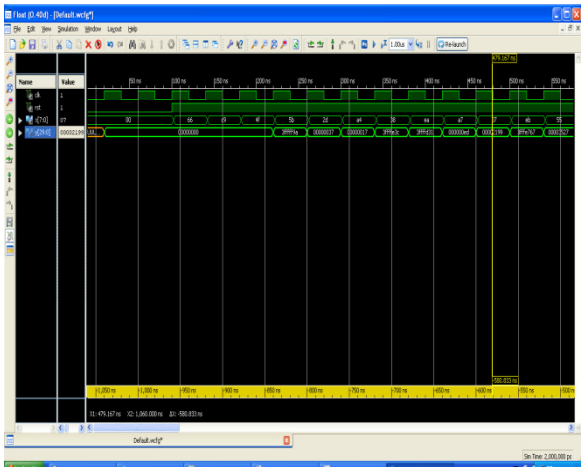

Fig 4: Output of transpose form FIR filter

Here we use transpose form FIR filter for both the fixed and reconfigurable applications. For fixed FIR filter there is a generalized formulation is present from that we derive multiplier based architecture for reconfigurable application because its coefficients are not constant they vary with run time.

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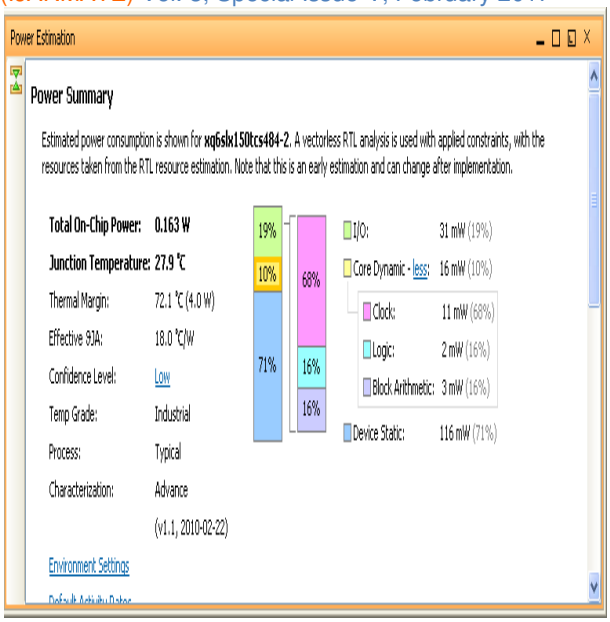

Fig 5: Power Estimation

Fig.5 shows the power estimation of the filter where the power estimation is less compared to existing system.

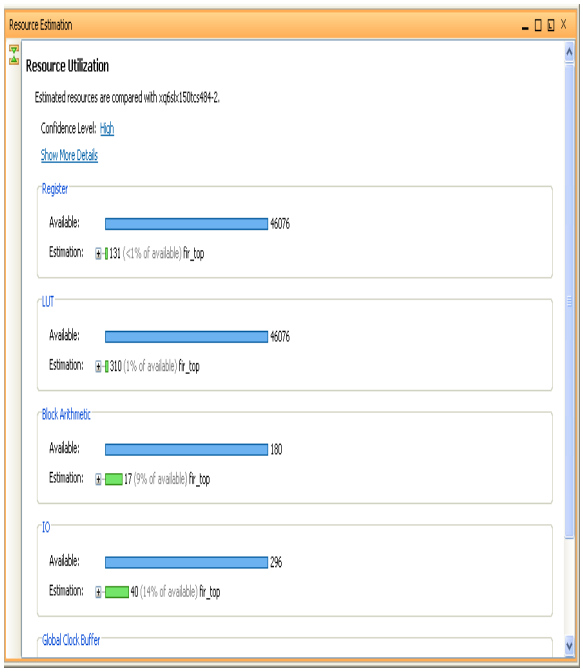

Fig 6: Resource Estimation

Fig .6 shows the resource estimation where the quantity of resources we have from that how much we used for this system.

VI. CONCLUSION

In this work we derive a chance to realize the transpose form configuration of block FIR filter for the fixed and reconfigurable application to provide area-delay efficiency.We have a generalized formulation for fixed FIR filter structure from that we derive multiplier based architecture for reconfigurable applications.If we use large and medium order filters in proposed structure that will provide less ADP and less EPS than the existing system.

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