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A New Topology For the Design of 3rd Order V-mode Universal Filter with 1 OTRA Using Alpha-Power Model

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***Abstract*—This paper proposes a multi-input single –output (MISO) third order voltage mode(VM) universal filter using only one Operational Transresistance Amplifier(OTRA).In the synthesis of transfer function the new topology of RC:-RC decomposition technique is used in the realization of an third order transfer function employing a single OTRA.The proposed circuit realizes low-pass,high-pass,all-pass,band-pass and notch responses from the new realized topology.The PSPICE simulation results using proteus8 professional technology agree well with the theoretical design.Design of this amplifier using Alpha-power MOS law model starts by the estimation of three unknown parameter α,Vth and k from the simulated I-V values of device characteristics,so that the simulated drain current should fit the Alpha-power based drain current equation.Proposed method is much simpler and fully technology independent and also free from complex mathematical expressions associated with the devices.**

Keywords—Operational Transresistance Amplifier,Transfer function synthesis,Alpha-power MOS law.

I. INTRODUCTION

The operational transresistance amplifier (OTRA), known also as a current differencing amplifier or Norton amplifier, is an important active element in analog integrated circuits and systems. Both input and output terminals of an OTRA are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The input terminals are internally grounded, leading to circuits that are insensitive to stray capacitances. Thus, it is possible to obtain very accurate transfer functions by using an OTRA in contrast to its unity-gain active device counterparts. Furthermore, it has a advantage of a high bandwidth and high slew rate. Some filter applications of an OTRA are present in the literature [1]-[8]. Also, realizations of n-th order transfer functions using OTRAs were reported a long time ago [9]-[12].To synthesize an n-th order transfer function, [9] and [10] need$n$+1 active elements, while [11] and [12] require n OTRAs. In this paper, we present a configuration that is suitable for a third order filter response, involving a single OTRA and the RC:−RC decomposition technique. This is a significant reduction in comparison with the previously reported configurations. In this work ,an attempt is made to design the third order voltage mode (VM) universal filter using the RC:-RC decomposition technique.Here,all the five filters like low pass filter(LPF),all pass filter(APF),band pass filter(BPF),high pass filter(HPF) and notch filter or band stop filter(BSF) are designed using the same topology.

II. PROPOSED CONFIGURATION

For the realization of the third order transfer function using Operational Transresistance Amplifier (OTRA),the equation of the OTRA is to be analysed with transimpedance gain and the input currents.Here, first the n-th order voltage mode transfer function is analysed with the single OTRA and then it is derived for the third order voltage mode transfer function. The general configuration to be used in the realization of an n-th order transfer function is shown in Fig. 1. With the following defining equations of an OTRA,

where R_m is the transresistance gain and ideally approaches to infinity forcing the input currents to be equal, the voltage transfer function of the network in Fig. 1 is found as

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{Y_a - Y_b}{Y_c - Y_d}, \qquad (2)$$

where Y_a, Y_b, Y_c and Y_d are positive real admittance functions of

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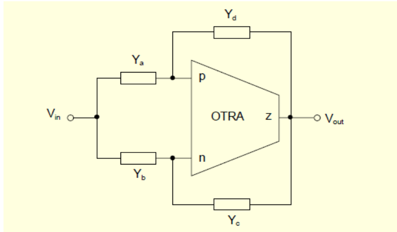

Fig. 1. Proposed configuration.

passive two-terminal elements. One of their terminals is internally grounded due to input properties of an OTRA. In the literature, a current-differencing buffered-amplifier-based n-th order current transfer function is realized using the same transfer function as (2) [13].

The form of $T(s)$ in (2) and the RC:−RC decomposition technique prove that the proposed configuration can realize any voltage transfer function of the form

$$T(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{a_m s^m+a_{m-1}s^{m-1}+\cdots+a_1 s+a_0}{b_n s^n+b_{n-1}s^{n-1}+\cdots+b_1 s+b_0}, \quad (3)$$

where $m \le n$ and a_i's and b_i's are real constants indicating coefficients of numerator and denominator polynomials, respectively. Note that to realize the prescribed transfer function $T(s)$ of (3), we write

$$T(s)=\frac{A(s)}{B(s)}=\frac{A(s)/D(s)}{B(s)/D(s)}, \quad (4)$$

where $D(s)$ is an arbitrary polynomial of degree n_D having only a simple negative real root, and where $n_D \ge \max(m,n) - 1$. Note that m and n are the degrees of the numerator and denominator polynomials, respectively [13].

III. DESIGN OF THIRD ORDER UNIVERSAL FILTER

As an example, a network for a third-order normalized all-pass function $T(s) = (-s^3+2s^2-2s+1) / (s^3+2s^2+2s+1)$ is obtained and simulated using the configuration in Fig. 1. In this design, the RC:−RC decomposition technique is used by choosing the arbitrary polynomial as D(s) = (s+1) (s+2). From (4), $T(s)$ can be written as

$$T(s)=\frac{(-s^3+2s^2-2s+1)/[(s+1)\,(s+2)]}{(s^3+2s^2+2s+1)/[(s+1)\,(s+2)]}. \quad (5)$$

Considering the transfer function of the proposed configuration given in (2) and equating its numerator to the numerator of (5) yields

$$\begin{aligned}Y_a - Y_b &= \frac{-s^3+2s^2-2s+1}{(s+1)(s+2)}\\ &= -s+5+\frac{6}{s+1}-\frac{21}{s+2}\\ &= -s+\frac{1}{2}+\left(-6+\frac{6}{s+1}\right)+\left(\frac{21}{2}-\frac{21}{s+2}\right)\\ &= -s+\frac{1}{2}-\frac{6s}{s+1}+\frac{21s}{2s+4}\\ &= \left(\frac{1}{2}+\frac{21s}{2s+4}\right)-\left(s+\frac{6s}{s+1}\right). \end{aligned} \quad (6)$$

From (6), the driving-point RC admittance functions are found as $Y_a = 1/2 + 21s/(2s+4)$ and $Y_b = s + 6s/(s+1)$. If the same procedure is applied for the denominators of (2) and (5), it is found that $Y_c = s + 1/2$ and $Y_d = 3s/(2s+4)$. The resulting third-order all-pass filter is shown in Fig. 2. Normalized values of passive components comprising the admittances are found as $R_{a1} = 2\ \Omega$, $R_{a2} = 2/21\ \Omega$, $C_a = 21/4$ F, $R_b = 1/6\ \Omega$, $C_{b1} = 1$ F, $C_{b2} = 6$ F, $R_c = 2\ \Omega$, $C_c = 1$ F, $R_d = 2/3\ \Omega$, and $C_d = 3/4$ F. If we choose the impedance scaling factor as 80×10^3 and the frequency scaling factor as $2\pi \times 100 \times 10^3$, the element values of the filter are calculated as $R_{a1} = 160$ kΩ, $R_{a2} = 7.619$ kΩ, $C_a = 104.445$ pF, $R_b = 13.333$ kΩ, $C_{b1} = 19.894$ pF, $C_{b2} = 119.366$ pF, $R_c = 160$ kΩ, $C_c = 19.894$ pF, $R_d = 53.333$ kΩ, and $C_d = 14.921$ pF. This choice leads to a resonant frequency of f_0=100 kHz.

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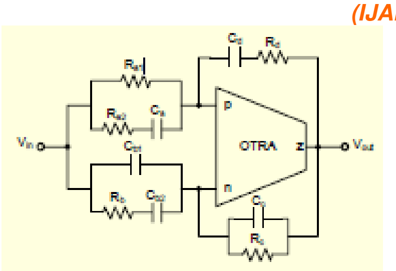

Fig. 2. Third-order all-pass filter.

As another example, a network for a third-order normalized low-pass function $T(s) = 1/(s^3+2s^2+2s+1)$ is obtained. In this design, using the RC:−RC decomposition technique again, the driving-point RC admittance functions are found as $Y_a = 1/2 + s/(2s+4)$, $Y_b = s/(s+1)$, and $Y_c = s + 1/2$, $Y_d = 3s/(2s+4)$ with the same arbitrary polynomial $D(s) = (s+1)(s+2)$. The resulting circuit is shown in Fig. 6. The element values of this filter are R_{a1} = 160 kΩ, R_{a2} = 160 kΩ, C_a = 4.974 pF, R_b = 80 kΩ, C_b = 19.894 pF, R_c = 160 kΩ, C_c = 19.894 pF, R_d = 53.333 kΩ,and C_d = 14.921 pF. This choice also leads to a resonant frequency of f_0 = 100 kHz.

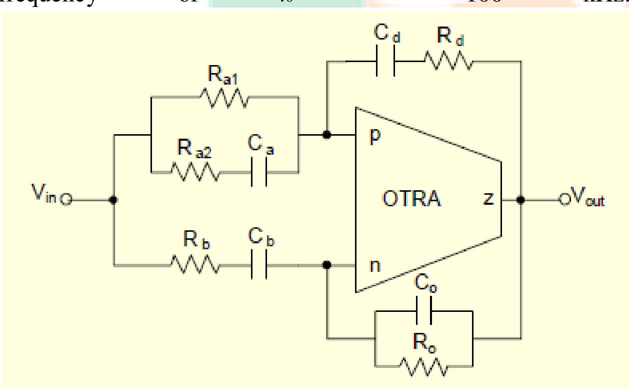

Fig:3 Third order low pass filter

Similarly, by designing for third order high pass filter, band pass filter and notch filter, we get the universal filter as

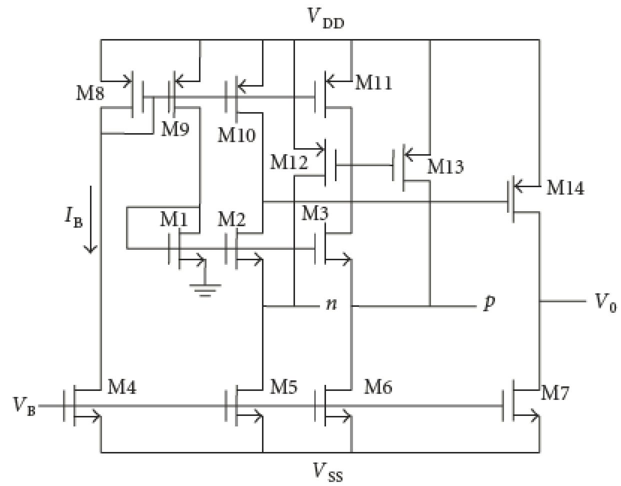

Figure:5 Internal circuit of OTRA

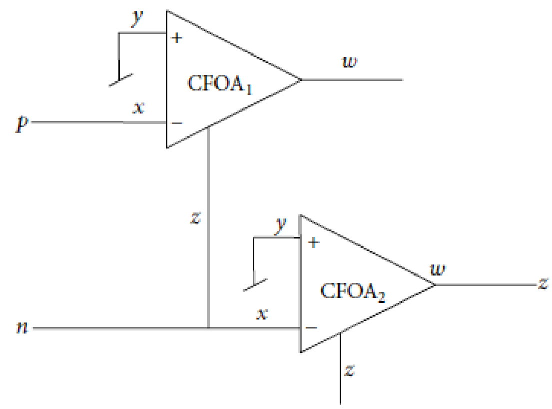

Figure:6 Implementation of OTRA using two CFOA's

Table 2:Design values of the passive components used for the third order voltage mode filters

Filter response	Component values										
	R_{a1} (kΩ)	C_{a1} (pF)	R_{a2} (kΩ)	C_{a2} (pF)	C_{b1} (pF)	R_b (kΩ)	C_{b2} (pF)	R_c (kΩ)	C_c (pF)	R_d (kΩ)	C_d (pF)
LPF	200	–	200	1.99	–	100	7.96	200	7.96	66.66	5.97
HPF	–	7.96	100	7.96	–	25	15.92	200	7.96	66.66	5.97
APF	200	–	9.52	41.79	7.96	16.66	47.76	200	7.96	66.66	5.97
BPF	–	–	50	7.96	–	100	7.96	200	7.96	66.66	5.97
NF	200	7.96	200	1.99	–	50	15.92	200	7.96	66.66	5.97

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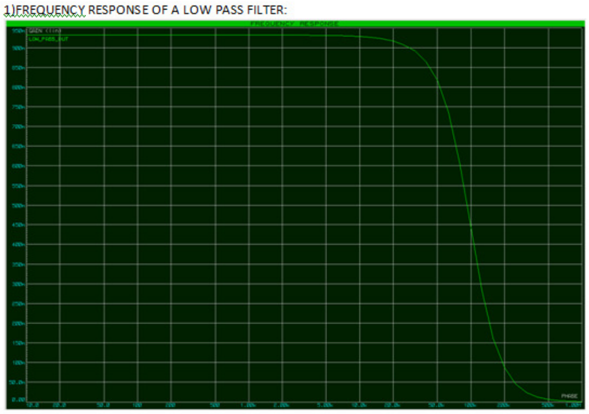
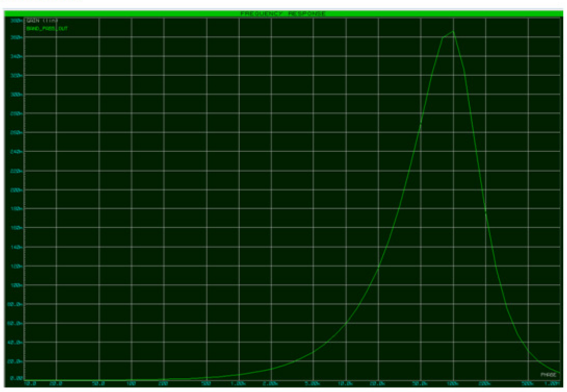
IV. SIMULATION RESULTS

The simulation is done by PSPICE technology using PROTEUS 8 professional.

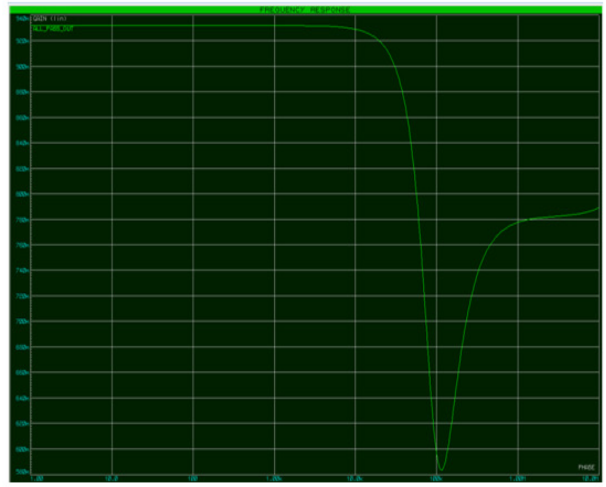
1)FREQUENCY RESPONSE OF A LOW PASS FILTER:



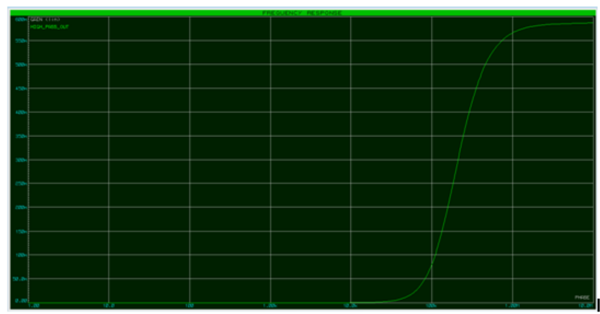
2)FREQUENCY RESPONSE OF A BAND PASS FILTER:



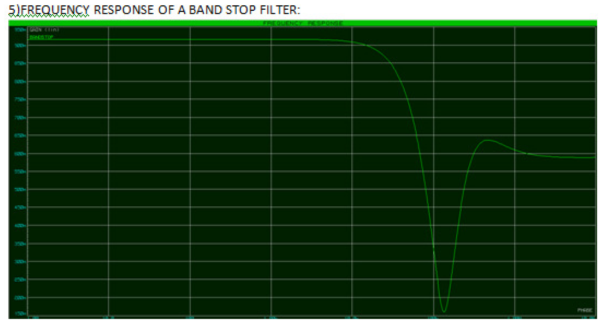
3)FREQUENCY RESPONSE OF A ALL PASS FILTER:



4)FREQUENCY RESPONSE OF A HIGH PASS FILTER:



5)FREQUENCY RESPONSE OF A BAND STOP FILTER:



V.DISCUSSION OF DESIGN PROCEDURE

In this section,the design of the amplifier in short channel MOSFET using alpha-power model is analysed.

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Alpha-Power model [4], in equation form is described below:

$$I_d = \begin{cases} 0 & : \text{Cutoff Region} \\ \dfrac{I'_{d0}}{V'_{d0}} & : \text{Linear Region} \\ I_{d0} & : \text{Saturation Region} \end{cases} \quad (1)$$

Where, $$I'_{d0} = I_{d0}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^{\alpha}$$

and $$V'_{d0} = V_{d0}\left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^{\frac{\alpha}{2}}$$

V_{d0} is drain saturation voltage at $V_{GS} = V_{DD}$ and I_{d0} is Drain current at $V_{GS} = V_{DS} = V_{DD}$. The simple drain current equation in saturation region ignoring CLM effect is:

$$I_d = k(V_{GS} - V_{TH})^{\alpha} \quad (2)$$

From (2) we can say drain current depends on three unknown parameter threshold voltage (V_{TH}), device transconductance (k) and velocity saturation index (α).

The section enlists proposed method based design procedure steps in details. Following are the design steps:

1. Estimate the unknown device parameters in equation (2) of a device dimension of width W and length L is the first and most important step to design an amplifier.

2. Using Potential Distribution Methodology (PDM) [9], we can easily calculate the required load resistance. If the supply voltage is V_{DD} and potential distributes equally on the transistor and resistor, then output DC will be at $V_{DS}=V_{DD}/2$. Therefore the required load resistance (R_{load}), for a bias current of I_{bias} becomes:

$$R_{load} = \frac{V_{DD} - V_{DS}}{I_{bias}} = \frac{V_{DD}}{2I_{bias}} \quad (4)$$

3. Generally, the gain equation of an amplifier with passive load (R_{load}) can be described as:

$$g_m R_{load} = A_V \quad (5)$$

From this general gain equation we can easily calculate the required g_m to satisfy all the design criteria without device output resistance (r_o) effect.

4. As, g_m of a SCM is lower than long channel MOSFET therefore we have to increase the device dimension to meet the required g_m. First check the bias voltage corresponds to bias current after modifying the device width using equation (6) with the full length gate voltage range (0-900mV) based α and k value. If the gate voltage range deviates from the previous range then modify the device width with the new α and k value according to new bias voltage falling region and check again. The modified device width will be the initial device width multiplied by a scaling factor (r) mention below:

$$r = \frac{1}{k} g_m (1-\alpha)\left(\frac{g_m}{\alpha}\right)^{\alpha} \quad (6)$$

5. If modified width and length be W' and L' respectively, then the aspect ratio becomes:

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$$\frac{W'}{L'} = r\left(\frac{W}{L}\right) \qquad (7)$$

6. Again check the biasing voltage V_{bias} corresponds to bias current I_{bias} if the falling region deviates from the previous one then according to new falling region of bias voltage repeat step 4 and 5 until α, k and V_{bias} tradeoff between each other achieved.

7. To achieve the required criteria, include drain to source resistance (r_o) in g_m calculation. After including (r_o) repeat step 4, 5 and 6. Simulation gives accurate result after including drain to source resistance and design error within acceptable limit (10%). Actual required $g_{m,req}$ will be:

$$g_{m,req} = A_v \left(R_{load} \parallel r_0\right) \qquad (8)$$

8. So, the final step is to set the device dimension by using the equations (5), (6) and (7).

VI.CONCLUSION

Thus the third order universal filter is designed in voltage mode(VM) using a single OTRA and the amplifier design procedure using alpha-power model is discussed.The simulation results are performed using the PSPICE technology of PROTEUS 8 professional tool.The design of the filter is done by the RC:-RC decomposition technique using a single OTRA.Therefore,it reduces a number of OTRA's compared to the previously reported ones.

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