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OPTIMIZED AREA DELAY AND POWER EFFICIENT CARRY SELECT ADDER USING NAND GATE

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Abstract:- Carry Select Adder is one of the fastest adders used in many data processing processors to perform fast arithmetic functions. Carry Select Adder requires larger area and power because of its internal structure which contains two Ripple Carry Adder and a multiplexer. The modern design system requires a reduction in size and less power consumption, this requirement is achieved in the Carry Select Adder. The logic operations involved in conventional Carry Select Adder and Binary to Excess-1(BEC) Converter based Carry Select Adder are analyzed to study the data dependence and to identify redundant logic operations. In this project, eliminated all the redundant logic operations present in the conventional Carry Select Adder and proposed a new logic formulation for Carry Select Adder. The additional power consumption can be reduced with the help of new logic formation technique using universal (NAND) gate. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families. Comparing NAND and NOR gate the NAND gate have better power performance.

Keywords: Adder, arithmetic unit, low-power design, universal gates, redundant logic, Binary to Excess-1converter.

I. Introduction

Low-power, area-efficient, and high-performance VLSI systems are increasingly used in portable and mobile devices, multistandard wireless receivers, and biomedical instrumentation. An adder is the main component of an arithmetic unit. Digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system. A ripple carry adder (RCA)[3] Uses a simple design, but carry propagation delay (CPD)[5] is the main concern in this adder. Look-ahead and carry select (CS) methods have been suggested to reduce the CPD of adders.

The Adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing, therefore its performance and power optimization is of utmost importance. With the technology scaling to deep submicron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to increasing density of chip. Therefore, in realizing modern VLSI circuits, low-power and high-speed are the two predominant factors which need to be considered.

Carry select adder is one of the types of fast adder. It can be implemented by using universal gate (NAND). A universal gate is a gate which can implement any type of Boolean function

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without need to use any other gate type. The NAND and NOR gate are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families. Comparing NAND and NOR gate the NAND gate have better power performance.

A. Linear Carry Select Adder

The Linear carry select adder is constructed by chaining a number of equal length adder stages. For an n-bit adder, it could be implemented with equal length of carry select adder and is called as linear carry select adder.

B. Square-root Carry Select Adder

The square-root carry select adder is constructed by equalizing the delay through two carry chains and the block multiplexer signal from previous stage. It is also called as non-linear carry select adder.

II. Existing Techniques

A. Regular carry select adder

The CSLA is used in many computational systems to alleviate the problem of carry propagate delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA[9]is not area efficient because it uses multiple pairs of RCA to generate partial sum and carry by considering carry input C_{in}=0 and C_{in}=1, then the final sum and carry are selected by the multiplexers.

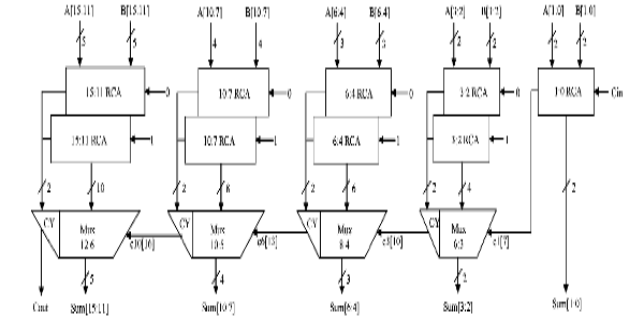

Figure 1: 16 bit Carry Select Adder

B. CSLA by using BEC technique

One input to the mux goes from the RCA with Cin=0 and other input from the BEC[10]. Comparing the both regular and modified (BEC) CSLA, it is clear that BEC structure reduces the area and power.But the disadvantage of BEC method is that the delay is increasing than the regular CSLA.

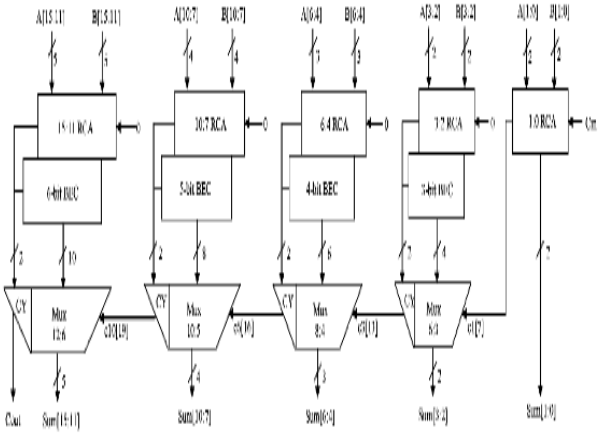

Figure 2: 16 bit Carry Select Adder

C. New Logic Formation Based CSLA

A 16 bit SQRT CSLA[1] design using the proposed CSLA is shown in Figure 3, where the 2-bit RCA, 2-bit CSLA, 3-bit CSLA, 4-bit CSLA, and 5-bit CSLA are used. Consider the cascaded configuration of (2-bit RCA and 2, 3,

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4, 6, 7, and 8-bit CSLAs) and (2-bit RCA and 2, 3, 4, 6, 7, 8, 9, 11, and 12-bit CSLAs), respectively for the 32-bit SQRT CSLA and the 64-bit SQRT CSLA to optimize Adder delay. To demonstrate the advantage of the CSLA design in SQRT CSLA, and estimated the area and delay of SQRT CSLA using the new logic formation CSLA design.

The multipath carry propagation feature of the CSLA is fully exploited in the SQRT CSLA, which is composed of a chain of CSLAs. CSLAs of increasing size are used in the SQRT CSLA to extract the maximum concurrence in the carry propagation path. Using the SQRT CSLA design, large-size Adders are implemented with significantly less delay than a single-stage CSLA of same size. However, carry propagation delay between the CSLA stages of SQRT CSLA is critical for the overall Adder delay. Due to early generation of output-carry with multipath carry propagation feature, the proposed CSLA design is more favorable than the existing CSLA designs for area–delay efficient implementation of SQRT CSLA.

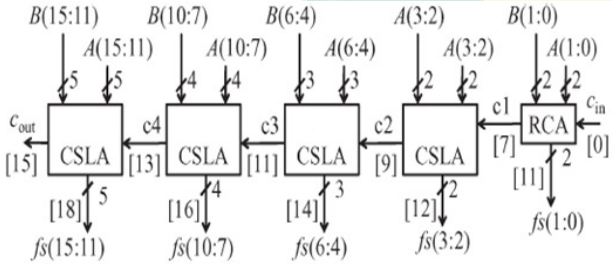

Figure 3: Block Diagram of 16 bit SQRT CSLA

The proposed CSLA is based on the logic formulation structure given is shown in Figure 3.2. It consists of one HSG unit, one FSG unit, one CG unit, and one CS unit. The CG unit is composed of two CGs (CG0 and CG1) corresponding to input-carry '0' and '1'. The HSG receives two n-bit operands (A and B) and generate half-sum word s0 and half-carry word c0 of width n bits each. Both CG0 and CG1 receive s0 and c0 from the HSG unit and generate two n-bit full-carry words c01 and c11 corresponding to input-carry '0' and '1', respectively.

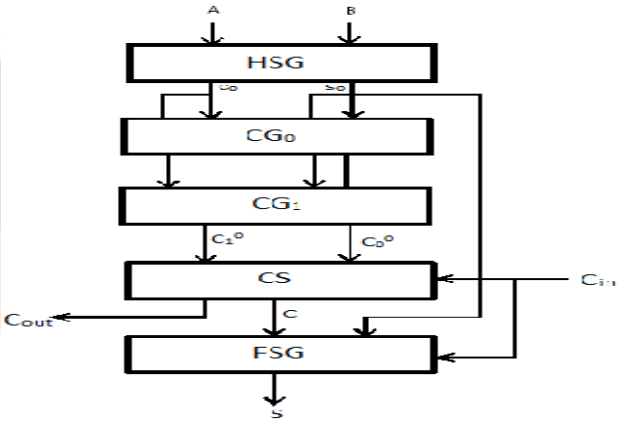

Figure 4: CSLA Design

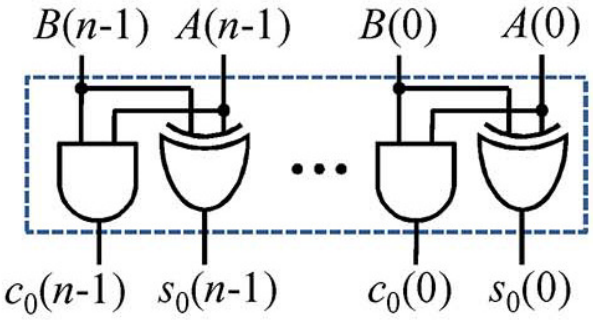

Figure 5: Design of HSG Unit

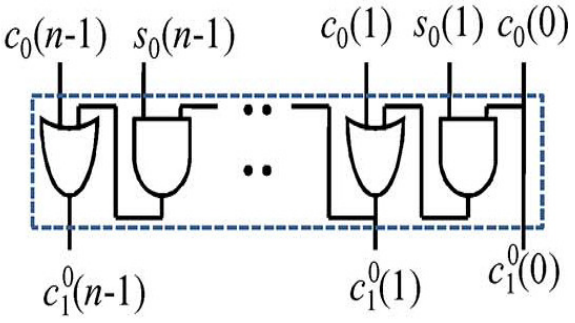

Figure 6: Design of CG0 Unit

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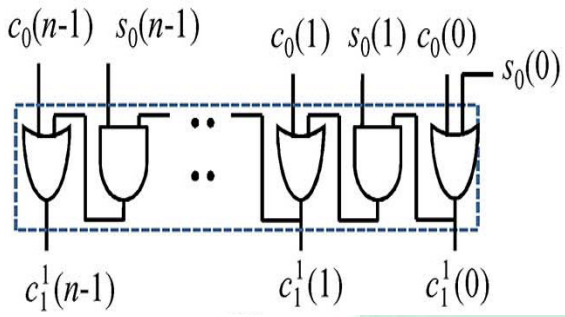

Figure 7: Design of CG1 Unit

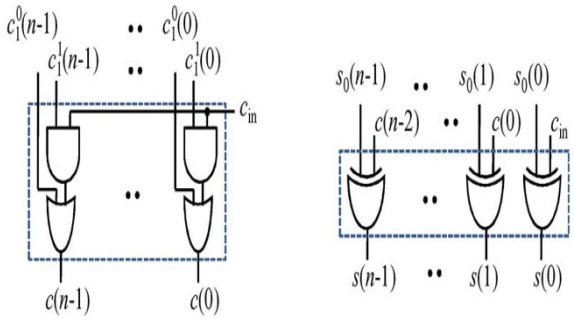

Figure 8: Design of CS and FSG Unit

III. Proposed CSLA Design

Optimized Area-Delay and Power Efficient Carry Select Adder is having all the features of Area-Delay-Power Efficient Carry Select Adder. Here the redundant logic operations of the system are identified and eliminated and new logic formulations are proposed for the system. Also the AND, OR and XOR logic used in the system is changed into a NAND based gates with optimal usage of FPGA resources. This substitution helps to reduce the area and power consumption of the whole system. Thus this carry select adder can be a good substitute for all the current adders and can be used in fast, power and area efficient devices.

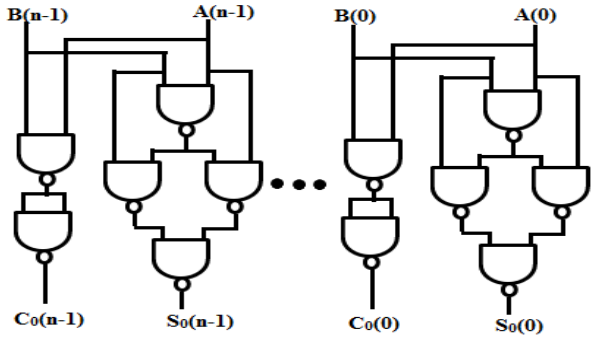

Figure 9: Modified Design of HSG Unit

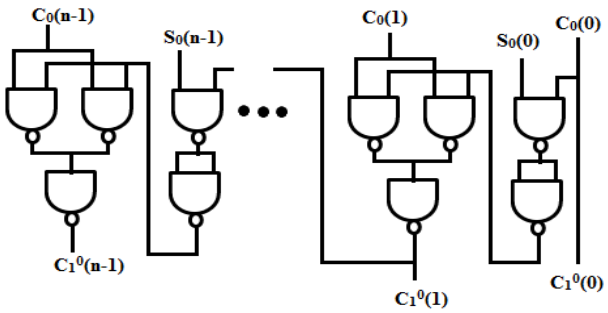

Figure 10: Modified Design of CS0 Unit

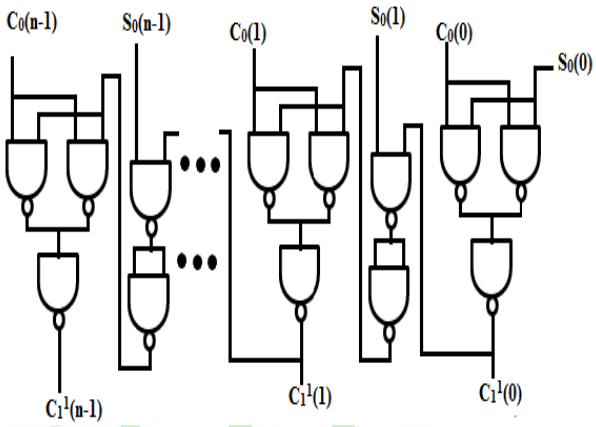

Figure 11: Modified Design of CS1 Unit

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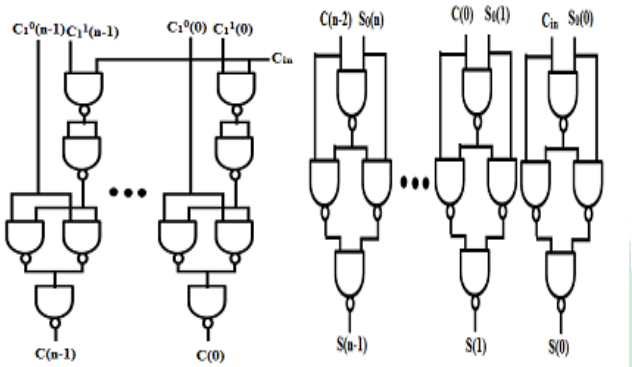

Figure 12: Modified Design of CS and FSG Unit

IV. Results and Discussion

The simulated results and the area delay and power analysis are discussed here. Xilinx 12.1 ISE (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of Hardware Description Language (HDL) designs, enabling to synthesis their design, perform timing analysis, examine Register Transfer Logic (RTL) diagrams, simulate a designer's reaction to different stimuli, and configure the target. Area analysis has done itself effectively.

A. Adder output

The Figure 5.4 shows that new logic formation output waveform of CSLA. The output of the circuit comes out according to the given input A=0100110011101010, B=0000001001001001 and Cin=1. And the corresponding binary output is Sout=0100111100110100.

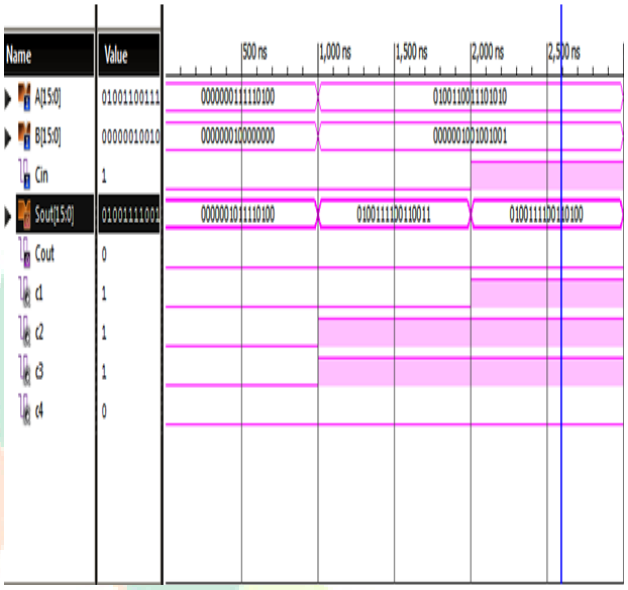

Figure 13: 16 bit CSLA Output

B. Area Utilization

By implementing the total system, the area consumed by the system is checked in the design summary. Thearea consumption is given in the terms of number of slices occupied. Fig shows the area utilization of the proposed system in an FPGA.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	32	1,920	2%	
Number of occupied Slices	19	960	2%	
Number of Slices containing only related logic	19	25	100%	
Number of Slices containing unrelated logic	0	25	0%	
Total Number of 4 input LUTs	32	1,920	2%	
Number of bonded IOBs	43	66	75%	
Average Fanout of Non-Clock Nets	1.9			

Figure 14: Area Utilization of 16 bit carry select adder

C. Power Consumption

The power consumption is the total power consumed by the system. The power

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consumption is also reduced. Thepower consumption is taken as a sum of leakage powerand dynamic power. Thus thetotal consumed power canbe obtained. Figure 15 shows the power consumption of theproposed system.

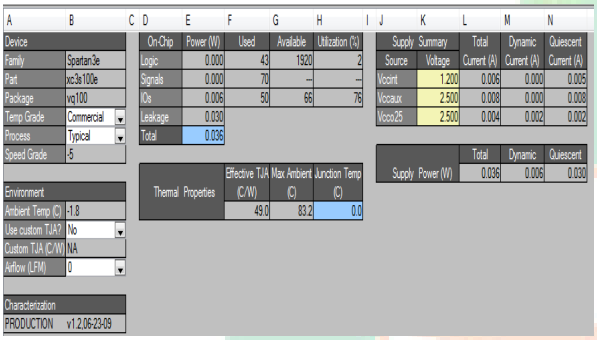

Figure 15: Power Consumption of 16 bit carry select adder

D. Timing Report

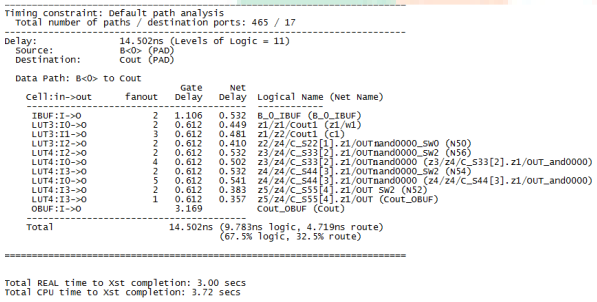

Figure 16: Timing report of 16 bit carry select adder

V. Performance Comparison

The results shows that the power consumption, area and delay of the system have been reduced comparing to previous systems. Table1 shows the comparison of the area, power and delay between existing and proposed carry select adders. Also the simulation of the system using NAND based gates instead of AND, OR, EX-OR gates shows a reduction in area and power consumption than the system using logic gates in FPGA. Thus the carry select adder proposed is having reduced area, power and delay consumption than existing adders.

Table1: Area and Power Consumption Comparison of Existingand Proposed Carry Select Adder

Design	Bits	Area (No Of Slices)	Power(w)		
			Total	Dynamic	Quiescent
CSLA using (AND, OR, Ex-OR)	16	24	0.039	0.006	0.034
CSLA using (NAND)	16	19	0.036	0.006	0.030

VI. Conclusion

A new logic formation design is introduced to achieve the area, delay and power efficient CSLA. All the redundant logic operations present in the conventional CSLA are eliminated and a new logic formulation for CSLA is introduced. In this technique carry select operation is scheduled before the calculation of final-sum, which is different from the conventional approach.

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