ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2, Special Issue 12, April 2016.

IMPLEMENTATION OF SRAM USING ULTRA LOW POWER TCAM

R. Keerthana,
PG Scholar,
P. A. College of Engineering and Technology, Coimbatore, India.
keerthana1192@gmail.com

Mrs. M. Madhumalini,
Assistant Professor of ECE
P. A. College of Engineering and Technology, Coimbatore, India.
madupavi.2007@gmail.com

Abstract- Static Random Access Memory plays a major role in many applications. Now a day's 9-Transistor multi-threshold Static Random Access Memory macro with equalized bit line leakage and a content-addressable- memory-assisted write performance boosting technique is used for energy efficiency improvement. In 9-Transistor Static Random Access Memory A 3- Transistors grouped to form a read port to equalize Read Bit Line leakage and to improve Read Bit line sensing margin by eliminating data-dependence on bit line leakage current. A miniature Content Addressable Memory-Assisted circuit is integrated to conceal the slow data development with High Voltage Threshold devices after data flipping in write operation and therefore enhance the write performance for energy efficiency. 9-Transistor Static Random Access Memory cell with equalized bit line leakage fosters Static Random Access Memory read operation at ultra-low voltage. Minimum energy of 2.07 PJ is achieved at 0.4 V with 40.3% improvement compared to the Static Random Access Memory Energy efficiency is enhanced by 29.4% by the proposed Content Addressable Memory-Assisted circuit. In order to reduce the power consumption further, Ternary Content Addressable Memory is used in many applications. When compared with Content Addressable Memory, Ternary Content Addressable Memory reduces 10% of power consumption.

Keywords: Bitline leakage equalization, Content addressable memory , Ultra - low voltage SRAM design, Ternary Content Addressable Memory.

SRAMs have achieved ultra-low power/energy through supply scaling. However, they suffer from various design issues mainly caused by reduced I_{on} -to- I_{off} ratio combined with large variations. Under severely scaled supply voltage, cell stability and bit line sensing margin of 6T SRAMs degrade dramatically due to the significant impact of disturbing current and bit line leakage. To handle it, an 8T differential SRAM cell has been proposed to inject identical leakage current into the differential bit lines, eliminating the differential offset voltage from the leakage. However, in general, decoupled SRAM cells are preferable in weak-inversion regime to make the read static-noise-margin (SNM) identical to the hold SNM. Moreover, the dedicated read port enables a faster read operation with no disturbing current to cell nodes.

Several design techniques are used to foster an energy efficient SRAM in a wide range of supply voltages with the following features: i) a decoupled 9T SRAM[2] cell with an improved SNM compared to the 6T cell; ii) a 3T read port for equalizing RBL leakage and augmenting bit line swing; iii) utilizing MTCMOS technology for minimizing leakage in 6T write part and maximizing SRAM performance in read port; iv) a CAM-assisted circuit technique for improving the energy efficiency by boosting the

All Rights Reserved @ 2016 IJARMATE

ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2, Special Issue 12, April 2016.

write speed. The proposed circuit techniques are demonstrated by a 16 kb SRAM test macro (including the CAM)[3] fabricated in a 65 nm CMOS technology.

Content-Addressable Memory (CAM) is a memory that implements the lookup-table function in a single clock cycle using dedicated comparison circuitry. Besides, Ternary Content-Addressable Memory (TCAM)[5] is one of Content-Addressable Memory (CAM). In this midterm will introduce the Content-Address Memory. TCAM is an important component for many applications especially for network. For TCAM-based networking system, the rapidly growing size of routing tables brings with it the challenge to design higher search speeds and lower power consumption.

II. EXISTING TECHNIQUE

A. CAM- Assisted 9T SRAM Circuit

The primary role of the CAM is to store most recent write addresses and data for possible subsequent read access till the data written into the main SRAM[2] array is fully developed. During write operation, data is written into the main SRAM array (through the SRAM write path) and the miniature SRAM array (through the CAM write path). The write address is stored in the CAM array. The write address and the data in the CAM can be accessed in the succeeding cycles since the proposed CAM is implemented with LVT devices. In Figure 1, During read operation, the main SRAM array is accessed for normal read operation, and the CAM array is simultaneously searched using the read address as search data. If the read address is not found in the CAM array, the cells that are written in the preceding cycles couldn't be accessed. Thus, the selection signal from the encoder will select the read data from the main SRAM array as the final data through MUX. If an address match occurs by a subsequent read-after-write operation, the encoder enables a word line signal corresponding to the matched address. 6

The word line activates reading data from the SRAM array and later the data is sent to MUX. Finally, using the selection signal from the encoder, MUX will select the data from the proposed CAM as the final data. In this case, the read data from the main SRAM array cannot be used as the final data since the data written in the previous cycle has not been fully developed due to the slow development speed of the latches using HVT devices. Therefore, the read data from the CAM should be selected as the final read data. Through this, the write performance is determined by the read operation or the data flipping delay, not by the slower full development delay. As a result, instant read-after-write operation for the same address is executable without slowing down the clock frequency for providing full data development in the main SRAM array.

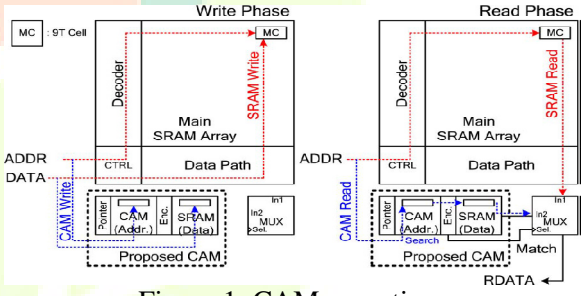

Figure 1: CAM operation

In the Figure 2 When a write operation is asserted, the pointer enables one row, writing the input address into the CAM array and the data into the miniature SRAM array. When a SRAM read operation is enabled, the address is loaded into the search lines (SL<i> and SLB<i>) of the CAM array. If the address is found from the CAM array, the corresponding ML(s) will be enabled. Otherwise, no ML is enabled and the search operation finishes. If multiple MLs are enabled, the encoder activates only one read word line CAM_RWL corresponding to the most recent write operation. The activated word line enables reading data through read bit lines CAM_RBL and sending the read data to MUX.

The energy dissipation by the proposed CAM circuit[3] occupies a very small portion of

All Rights Reserved @ 2016 IJARMATE

ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2, Special Issue 12, April 2016.

the overall consumption. Simulation shows that the CAM energy per read with search operation is 59 fJ at 0.4 V with frequency of 1 MHz To be more flexible, data from CAM_RBL and SRAM_RBL can bypass the MUX for separate measurement A 16 kb SRAM test chip is fabricated in a commercial 65 nm CMOS technology with a nominal V_{DD} of 1.2 V. Power of read and write operation is measured at the maximum operating frequency. The read power is larger than the write power due to the precharging and discharging current in the read bitlines. The average power is measured in the supply range of interest, assuming equal probability of performing read and write operations.

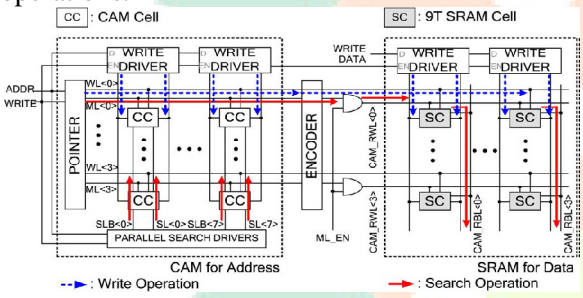

Figure 2: Block Diagram of CAM

B. CAM-assisted Write Performance Boosting Technique

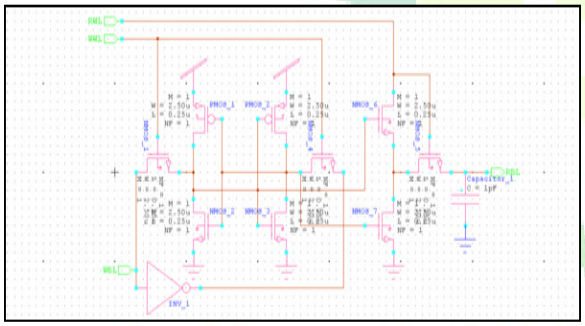

Figure 3: CAM Assisted SRAM Circuit

In Figure 3, The SRAM comprises two main paths, an SRAM path and a CAM path. The SRAM path consists of a 16 kb 9T SRAM array (main SRAM array), decoders and data IOs. The CAM path is composed of a tiny 48 b CAM array for storing addresses, a ring counter as an address pointer, an encoder, and a miniature SRAM array for storing write data. The CAM array (Address) and the SRAM array (Data) are implemented with LVT devices for faster read, write, and parallel search to conceal the slow full data development in the main SRAM array.

The primary role of the CAM is to store most recent write addresses and data for possible subsequent read access till the data written into the main SRAM array is fully developed. During write operation, data is written into the main SRAM array (through the SRAM write path) and the miniature SRAM array (through the CAM write path). The write address is stored in the CAM array. The write address and the data in the CAM can be accessed in the succeeding cycles since the proposed CAM is implemented with LVT devices.

III. PROPOSED TECHNIQUE

A. Basic Flow of TCAM

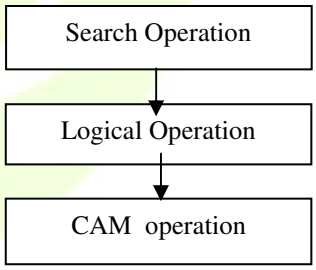

Figure 4: Flow of TCAM operation

In TCAM[5] Three operations will take place. They are Search operation, Logical Operation and CAM operation. Search and CAM operations are identical to both CAM and TCAM. But the logical operation is carry out only in the TCAM cell. This is the main Difference between the CAM and TCAM. And in CAM only two values can be processed (0's and 1's), But in TCAM one additional value can be process ((X) don't care value) The NOR and NAND cells that have been presented are binary CAM cells. Such cells store either logic "0" or

All Rights Reserved @ 2016 IJARMATE

ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2, Special Issue 12, April 2016.

logic "1". Ternary cells, in addition, store an "X" value. The "X" value is a don't care, that represents both "0" and "1", allowing a wildcard operation. Wildcard operation means that an "X" value stored in a cell causes a match regardless of the input bit.

B. Proposed NOR Type CAM cell

TCAM cell consisting two types of cells. They are NOR type and NAND type cell. In NOR type cell the search transistors are connected in series with the latches. So when compare with normal CAM cell it additionally performs logical operation. But NOR based TCAM consume more power when compared with normal CAM it is proved by the analysis.

TCAM provides single clock lookup, however, it has several disadvantages compared with SRAM. TCAM is not subjected to the intense commercial competition found in the RAM market. TCAM cell adds complexity to the TCAM architecture.

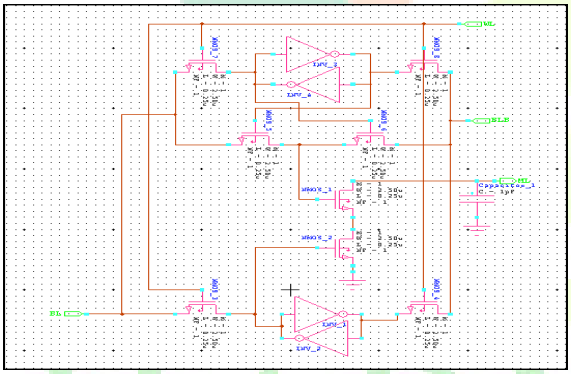

Figure 5: NOR Type TCAM

C. Proposed NAND Type TCAM

In NAND based TCAM, search transistors are connected in parallel manner. And it consumes only less power when compare with NOR based TCAM and normal CAM. So this NAND based TCAM is used in many applications like computer routers.

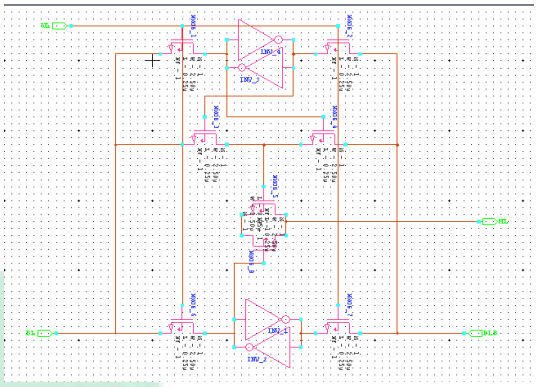

Figure 6: NAND Type TCAM

D. 8 X 8 NAND Type TCAM

Single bit TCAMs are connected in series manner to form the 64 bit memory(TCAM). This memory is used to store 64 redundant bits. The main difference between the normal CAM and TCAM is in TCAM the over writing operation is avoided. So this is used applications such as Network routers.

IV. RESULTS AND DISCUSSIONS

The proposed circuit is simulated using Tanner in the high-performance 180-nm technology. The supply voltage used in the simulation is 1.8 V. S-Edit is a schematic capture tool that supports integrated analog simulation with automatic conversion from cadence and view draw schematics. Users can run simulations and cross-probe from S-Edit, making the design process real-time and more efficient.

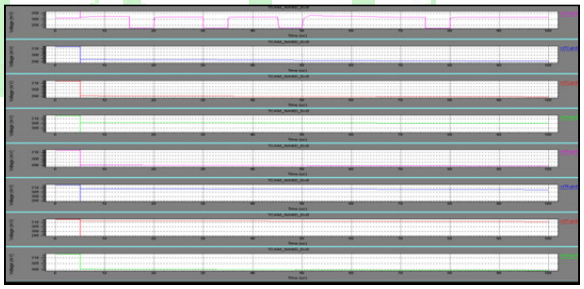

Figure 7: Simulation Result for the 8 X 8 NAND Type TCAM

All Rights Reserved @ 2016 IJARMATE

ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2, Special Issue 12, April 2016.

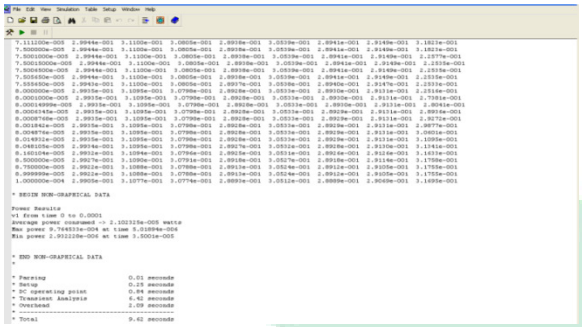

Figure 8: Power Report of 8 X 8 NAND Type TCAM

Table 1: Power Comparison Table

STRUCTURE	9T SRAM	CAM	NOR Type TCAM	NAND Type TCAM
Technology CMOS	130nm	130nm	130nm	130nm
Supply Voltage	1.8V	1.8V	1.8V	1.8V
Power Consumption	1.728767e-004 Watts	1.004008 Watts	7.09e-008 Watts	1.15e-009 Watts

A. Static Power Consumption

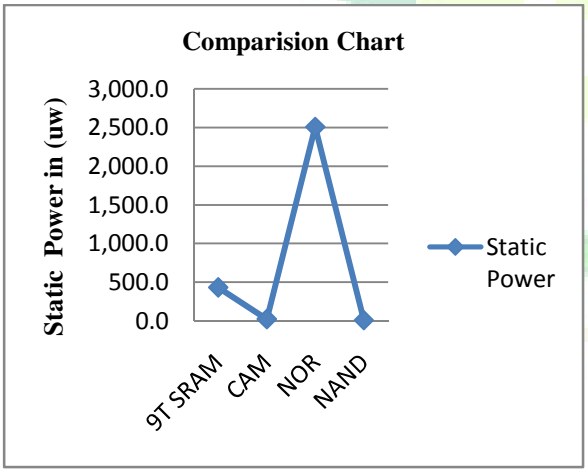

Figure 9: Comparison of Static Power

B. Average Power Consumption

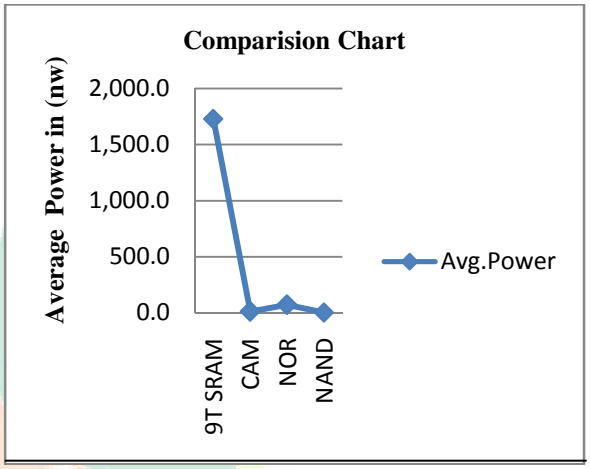

Figure 10: Comparison of Average Power

V. CONCLUSION

Leakage and energy efficiency are primary concerns for ultra-low voltage SRAM design. CAM technique is used to implement an energy efficient SRAM with reliable read operation under ultra-low voltage. 9T SRAM cell with equalized bit line leakage fosters SRAM read operation at ultra-low voltage, achieving read access time of 79 ns at 0.4 V and 0.85 s at 0.26 V, respectively. And a CAM-assisted write performance boosting circuit is used to speed up clock frequency. The test chip shows an average performance improvement of 29.4% with the aid of the proposed circuit technique. For further reduction of power consumption TCAM technique is used here. Because of don't care value the over writing operation is avoided which is happened in normal CAM.

REFERENCES

[1] Bo Wang, Truc Quynh Nguyen (2015), 'Design of an Ultra-low Voltage 9T SRAM With Equalized Bitline Leakage and CAM-Assisted Energy Efficiency Improvement', IEEE transactions on circuits and systems—I: regular papers, Vol. 62, No. 2.

All Rights Reserved @ 2016 IJARMATE

ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2, Special Issue 12, April 2016.

[2] Adam Teman, Lidor Pergament, Omer Cohen, and Alexander Fish (2011) , 'A 250 mV 8 kb 40 nm Ultra-Low Power 9T Supply Feedback SRAM (SF-SRAM)', IEEE journal of solid-state circuits, Vol. 46, No. 11.

[3] Banit Agrawal, and Timothy Sherwood (2008), 'Ternary CAM Power and Delay Model Extensions and Uses', IEEE transactions on very large scale integration (vlsi) systems, Vol.16, No. 5.

[4] Benton Highsmith Calhoun, Anantha and Chandrakasan (2007), 'A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation', IEEE journal of solid-state circuits, Vol. 42, No. 3..

[5] Chiao-Ying Huang (2012), 'Ternary Content-Addressable Memory Circuits' Midterm Report – IEE5009: Memory System , Institute of Electronics, National Chiao-Tung University.

[6] Dongsuk Jeon , Mingoo Seok, Chaitali Chakrabarti and David Blaauw (2012), 'A Super-Pipelined Energy Efficient Subthreshold 240 MS/s FFT Core in 65 nm CMOS', IEEE journal of solid-state circuits, Vol. 47, No. 1.

[7] Hong-YunKim,Young-JunKim, Jie-Hwan Oh, , and Lee-Sup Kim (2013), 'A Reconfigurable SIMT Processor for Mobile Ray Tracing With Contention Reduction in Shared Memory', IEEE transactions on circuits and systems—I: regular papers, Vol. 60, No. 4 .

[8] Ik Joon Chang, Jae-Joon Kim, Sang Phill Park and Kaushik Roy (2009), 'A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS', IEEE journal of solid-state circuits, Vol. 44, No. 2.

[9] Jayalakshmi Devi and Dr.satyanarayana (2014), 'VLSI Design of Power Gated NOR-based Content Addressable Memory' IJSRM Volume 2.

[10] KostasPagiamtzis andAli Sheikholeslami (2006), 'Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey' , IEEE journal of solid-state circuits, Vol. 41.

[11] Ming-Hsien Tu, Jihi-Yu Lin, Ming-Chien Tsai (2012), 'A Single-Ended Disturb-Free 9T Subthreshold SRAM With Cross-Point Data-Aware Write Word-Line Structure, Negative Bit-Line, and Adaptive Read Operation Timing Tracing', IEEE journal of solid-state circuits, Vol. 47.

[12] MohammadHassan Ghaed, GregoryChen (2013), 'Circuits for a Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor', IEEE transactions on circuits and systems-I: regular papers, Vol. 60, No. 12.

[13] Scott Hanson, Mingoo Seok, Yu-Shiang Lin, ZhiYoong Foo, Daeyeon Kim, and Yoonmyung Lee (2009) 'A Low-Voltage Processor for Sensing Applications With Picowatt Standby Mode' IEEE journal of solid-state circuits, Vol. 44, No. 4.

[14] Singh.R.K,Manisha Pattanaik, Neeraj Kr. Shukla, S.Birla and Sveen Nagpal (2012), 'Analysis and Simulation of a Low-Leakage 10T SRAM Bit-Cell using Dual-Vth Scheme at Deep Sub-Micron CMOS Technology' Proc. of the Intl. Conf. on Advances in Electronics, Electrical and Computer Science Engineering - EEC.

[15] Tae-Hyoung Kim, Jason Liu, andChris H. Kim (2009), 'A Voltage Scalable 0.26 V, 64 kb 8T SRAM With V_{min} Lowering Techniques and Deep Sleep Mode', IEEE

All Rights Reserved @ 2016 IJARMATE