DESIGN AND ANALYSIS OF 1-BIT MEMORY CELL USING GRAPHENE NANORIBBON

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ABSTRACT- In the world of Integrated circuits, Complementary Metal-Oxide-Semiconductor (CMOS) technology has lost its credentiality during scaling beyond 32nm. Scaling causes severe Short Channel Effects (SCE) which are difficult to suppress. As a result of such effects, many alternate devices have been studied. Some of the major contestants include Multi Gate Field Effect Transistor (MuGFET) like FinFET, Carbon Nano tubes, Graphene Nano Ribbon, silicon Nano wires etc. Among these, Graphene Nanoribbon plays a vital role in modern electronic design. In this paper, the CMOS transistors present in the 1 bit SRAM memory cell is replaced by GNRFETs. The performance of SRAM memory cell built by 32nm GNRFET technology is compared with CMOS,FinFET and CNTFET technology using HSPICE simulation tool.

Keywords: Carbon Nanotube, Graphene Nanoribbon, Power dissipation.

1. INTRODUCTION

Semiconductor memories are most vital microelectronic components of digital logic system design, such as computers based application ranging from satellites to consumer electronics. Semiconductor memory arrays are capable of storing large quantities of digital information which are essential for all digital systems. The amount of memory required in a particular system depends on the type of application, but the number of transistors required for storage function is larger than for logic operations and other applications. The ever increasing demand for large storage capacity has driven the fabrication technology and memory development towards higher data storage densities. On-chip memory arrays have become widely used subsystems in VLSI circuits and commercially available single chip read/write memory capacity has reached 1 GB.

The semiconductor memory is generally classified according to the type of data storage and data access. Read/write memory or Random access Memory (RAM) must permit the change of data bits stored in the memory array, as well as their retrieval demand. The stored data is volatile.

In modern age people in the electronic industry commonly use the term “memory” to refer to RAM. A computer uses RAM to temporarily hold instructions and data necessary for the CPU to process tasks. In networking equipment, memory is used to buffer various types of information. Based on the operation type of individual data storage cells, RAMS are classified in to two main catagories: Dynamic RAM (DRAM) and Static RAM (SRAM).

The SRAM consists of latch so the cell data is kept as long as power is turned ON and refresh operation is not required. The DRAM cell consists of a capacitor to store binary information and a transistor to access the capacitor. The cell data must be read and rewritten periodically even when memory arrays are not accessed.

DRAM is widely used for main memory in personal and mainframe computers and engineering workstations. SRAM is mainly used for cache memory in microprocessor, mainframe computers, engineering workstations and memory in handled devices due to high speed and low power consumption. Memory cells are constructed using transistors. Even though they provide high speed of operation, lower leakage and reduced transistor count, they become less efficient when the area decreases below 32nm.

In this paper, the transistors in the SRAM cells are replaced by Graphene Nanoribbon, to reduce power consumption and the simulation is done by using HSPICE tool. The simulation results of GNRFET-SRAM are compared with the simulation results of CMOS SRAM on the basis of power dissipation.

2. LITERATURE SURVEY

Many researches are being carried out in the field of SRAM. Newer technologies are coming to existence. Moore’s law states that the number of transistors per square inch in an integrated circuits doubles every eighteen months but now the law is facing certain discrepancies, [2]. In the existing system, SRAM memory cells are designed using CMOS technology,[4]. It has various advantages like the circuit is very simple, consumes little power in a fixed state and also has high input impedance. Though it has these advantages, it fails when it is scaled beyond 32nm. It undergoes Short Channel Effect which is an effect whereby a MOSFET in which the channel length is the same order of magnitude as the depletion-layer widths of the source and drain

junction, behaves differently from other MOSFETs. . As a result of this short channel effects, the power dissipated by CMOS SRAM circuit becomes very high below 32nm. The read stability and write ability are major concerns in nanoscale.

3. GRAPHENE NANORIBBON

Graphene Nanoribbon is also called as nano-graphite ribbons, are strips of graphene with ultra-thin width (<50nm). Graphene ribbons were introduced as a theoretical model by Mitsutaka Fujita and co-authors to examine the edge and nanoscale size effect in grapheme,[1]. Careful patterning of graphene laterally confined in ribbon like structure gives rise to Graphene Nanoribbons (GNRs).

They are of two types- armchair and zigzag. In Zigzag, each segment is of opposite angle to the previous. In armchair type, each pair of segments is a 120/-120 degree rotation of the prior pair,[5]. Zigzag edges provide the edge localized state with non-bonding molecular orbitals near the Fermi energy. They are expected to have large changes in optical and electronic properties from quantization.

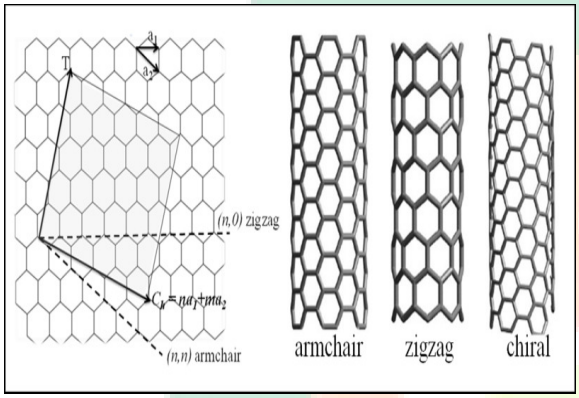

Figure 1: Graphene Nanoribbon

Calculations based on tight binding theory predict that zigzag GNRs are always metallicwhile armchairs can be either metallic or semiconducting, depending on their width. Density Function Theory (DFT) calculations show that armchair nanoribbon are semiconducting with an energy gap scaling with the inverse of the width of Graphene Nanoribbon. Experiments verified that energy gaps increase with decreasing GNR width,[8].

Graphene Nanoribbons possess excellent semiconductive properties and may be used as an alternative for silicon semiconductor. Their 2D structure along with certain properties like high electrical and thermal conductivity makes GNR an alternative to copper for Intergratedcircuits interconnect.

3. ALTERNATIVE-CARBON NANOTUBES

Carbon Nanotubes are tubular cylinders of carbon atoms that have extraordinary mechanical, electrical, thermal, optical and chemical properties. They are of two types which are single walled and multi walled Carbon Nanotubes,[4]. The nanotubes exhibit unique structures like 200X the strength, 5X the electrical conductivity and 5X the elasticity of steel.CNTFET (Carbon Nanotube Field Effect Transistor) utilizes a single carbon Nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure.

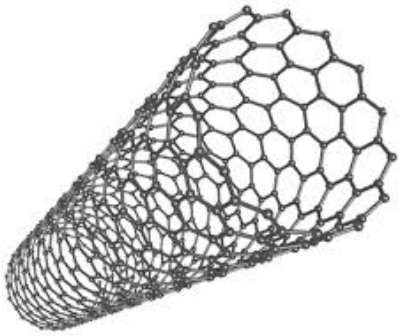

Figure 2: Carbon Nanotube Structure

Based on their folding angle and diameter, these nanotubes can be metallic or semiconductive. The band gap of semiconducting nanotubes decreases with increase in diameter. Electronic structure of carbon nanotubes makes then ideal candidates for novel molecular devices, [5].This can also be used as an alternative for CMOS technology beyond 32nm in order to overcome its short comings.

4. SRAM CELL

SRAM stands Static Random Access Memory. It finds application in CPU Cache, Personal Computers, workstations, routers, hard disk buffers and router buffers. The advantage of SRAM is that it does not require periodic refreshment unlike DRAM. It is also volatile i.e. the data is lost once the power is turned off. The construction of a 6T SRAM cell consists of 2 PMOS and 4 NMOS transistors.

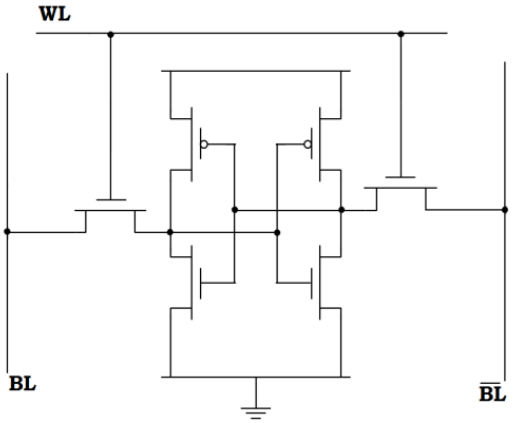

Figure 3: 6T SRAM CELL

The operation of SRAM cell is explained by considering 6T SRAM cell as an example, [7]. From the figure 3 we can understand the circuit diagram of 6T SRAM cell. The operation of SRAM can be divided into three states: read, write and hold state. During write operation, the voltage of WL is increased and Bit lines BL and BL' are raised to Vdd or with necessary values. The new bit line value overpowers the existing value. During read operation, the WL voltage is raised high, the memory cell discharges either BL or BL' depending on the storeddate on the nodes Q and Q'. During Hold state, the voltage in WL is held low and the BLs are left floating or driven to Vdd.

Each bit in an SRAM is stored on four transistors that form two cross-coupled. This storage cell has two stable states, which are used to denote 0 and 1. Two additional access transistors control the access to storage cell during read and write operation.

4. SIMULATION

Hailey's Simulation Program with Intergrated Circuit Emphasis (HSPICE) is software that supports the simulation of SRAM cell using Graphene Nanoribbon. Simulations are carried out to measure the power dissipated by CMOS and GNRFET (Graphene Nanoribbon Field Effect Transistor). Along with this, the power dissipated by CNTFET is also estimated and results are tabulated to find the technology that has minimum power dissipation below 32nm.

The simulation result of 6T SRAM cell is shown below and the same is obtained for various technologies used. The first waveform represents the word line, the second waveform represents the bit line and third waveform represents the output depending on whether it is read or write operation.

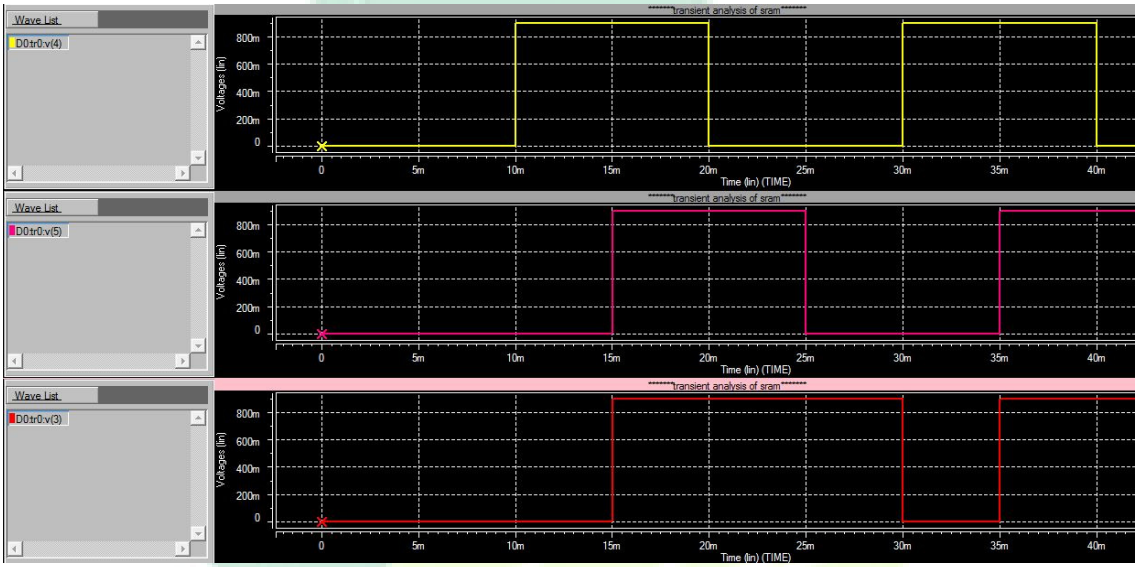

Figure 4: Simulation Waveform of 6T SRAM cell

5. COMPARISON TABLE:

DESIGN TECHNOLOGY	POWER DISSIPATION
CMOS	5.5079 e-9 W
CNTFET	3.290 e-11 W
GNRFET	6.834 e-11 W

6. CONCLUSION:

From this it can be concluded that, though CMOS is irreplaceable, the power dissipated by GNRFET is comparatively less than CMOS. The power dissipated by CNTFET is also less than CMOS beyond 32nm. The circuit designed using GNRFET is more efficient than CMOS technology beyond 32nm. The scope of Graphene Nanoribbon in the field of VLSI proves to be promising and paves way for a new revolution in MOSFET technology. Graphene Nanoribbon can thus be used as an alternative for CMOS beyond 32nm.

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