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Implementation of High Speed Low Power Split-SAR ADCs

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ABSTRACT: This paper analyzes the parasitic effects in SAR ADCs. Successive approximation technique in ADC is well known logic, where in the presented design the linearity analysis of a Successive Approximation Registers (SAR) Analog-to-Digital Converter (ADC) with split DAC structure based on two switching methods: V_{CM} -based switching, Switch to switchback process. The main motivation is to implement design of capacitor array DAC and achieve high speed with medium resolution using 45nm technology. The other advantage is matching of capacitor can be achieved better then resistor. This is verified by behavioural Measurement results of power, speed, resolution, and linearity clearly show the benefits of using V_{CM}-based switching. In the proposed design the SAR ADC is designed in switch to switchback process such a way that the control modules completely controls the splitting up of modules, and give an option to change the speed of operation using low level input bits. A dedicated multiplexer is designed for that purpose system.

KEYWORDS: Linearity analysis, linearity calibration, resolution SAR ADCs, split DAC, V_{CM}-based switching, Capacitor Based Switching.

I.INTRODUCTION

1.1 Selection of the right ADC architecture

The selection of the right architecture is a very crucial decision. The following figure 1 shows the common ADC (Analog to Digital Converter) architectures, their applications, resolutions and sampling rates. Sigma Delta ADC architectures are very useful for lower Sampling rate and higher resolution (approximately 12-24 bits). The common applications,for Sigma-delta ADC architecture are found in voice band, audio, industrial measurements and suitable for data acquisition.

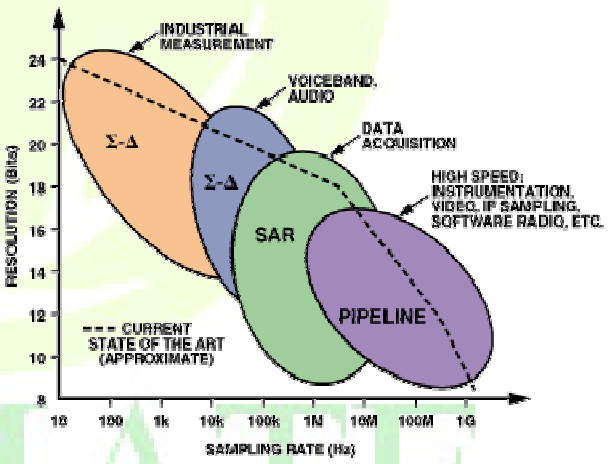

Fig.1 ADC architecture, applications, resolution, and sampling rate.

1.2. SAR ADC Architecture

The SAR architecture mainly uses the binary search algorithm. The SAR ADC consists of fewer blocks such as one comparator, one DAC and one control logic. The algorithm is very similar to like searching a number from telephone book. For example, to search a telephone number from telephone book, first the book is opened and the number may be located either in first half or in the second half of the book. This procedure can be followed until finding relevant number. The SAR ADC has compact design compare to flash ADC, which makes SAR ADC inexpensive. The physical limitation of SAR ADC is, it has one comparator throughout the entire conversation process.

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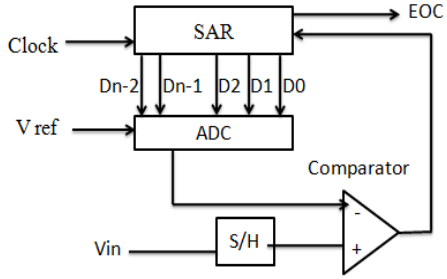

Fig. 2 block diagram of SAR ADC

II. EXISTING SYSTEM

2.1 V_{CM} Based Switching

The V_{CM}-based approach performs the MSB transition by connecting the differential arrays to V_{CM}.The power dissipation is just derived from what is needed to drive the bottom-plate parasitic of the capacitive arrays, while in the conventional charge-redistribution where the necessary MSB "up" transition costs significant switching energy and settling time. Therefore, the next $n-1$ b estimation is done with an $(n-1)$ bit array instead of its n-bit counterpart.

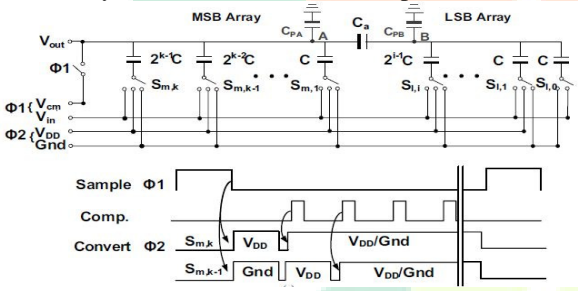

Fig 3(a)Conventional Switching

The comparator output predicts the switching logic for the MSB capacitor. If Out_ {comp} results low simulation, k is switched back to Gnd. If Out_ {comp} becomes high, then simulation, k maintained V_{DD}. The above process repeats forn – 1 cycle. V_{CM}-based switching after (n – 1) bit cycling, the DACs will finally settle to a value for LSBs decision. The differential DAC output is quite sensitive to supply variations, especially in the most critical case where the bottom plates of all the DAC capacitors (on the signal side) are connected to V_{DD}. Since the operation is differential, considering one of the corresponding cases: all bits in Vop1 are "1" and all bits in Von1 are "0," the differential output Vout of the DACs can be represented as,

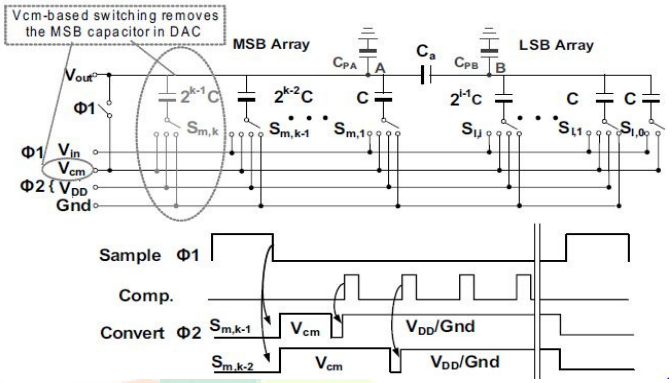

Fig. 3(b) V_{CM}-Based Switching

$$V_{OUT} = V_{OP1} - V_{ON1}$$

$$Vout = \left[\frac{2^{n-1}-1}{2^{n-1}}(V_{DD}+\Delta V) + \frac{1}{2^{N-1}}V_{CM}\right] - \frac{1}{2^{N-1}}V_{CM}$$

V_{CM}-based switching prevents occurrence of such large switching transient. In every bit cycle, only one capacitor is switched to obtain a voltage value by successive approximation of the input voltage without wasting energy and settling time.

III. PROPOSED SYSTEM

In the proposed system we are planning to implement SAR ADC in a configurable manner with different frequency inputs, the configurable means that the entire ADC architecture can work with different perfromance by changing the Vref of the ADC. Normally in all ADC Vref , Vin , Vth plays. A major role in adc conversion, by varying the values of Vref. we can change the performance of the ADC, We store the different values of Vref through Multiplexer , for selecting the mux inputs we have counter, Reference signal generator generates different analog signals to to test our ADC .

SAR ADCs provide a high degree of configurability on both circuit level and architectural level. At architectural level the loop order and

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oversampling ratio can be changed, the number of included blocks, and way these blocks are arranged. At circuit level many things could change, such as bias currents, amplifier performance, quantized resolution etc.

3.1 BLOCK DIAGRAM

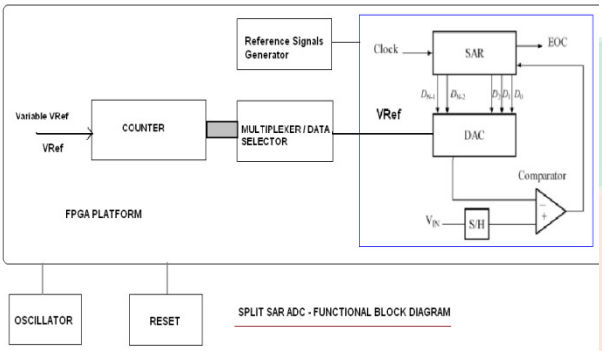

Fig.4 Major Block Diagram for Split-SAR ADC with FPGA

If an ADC is reconfigured in the way the blocks in the ADC are used and ordered, it is an architectural change of the ADC, or architectural re configurability. These blocks can also be changed, for instance how the amplifiers are biased, or how many bits of resolution that a quantise has in a SAR ADC.These are examples of how circuit level reconfigurability is applied to an ADC.If an ADC is reconfigured in the way the blocks in the ADC are used and ordered,it is an architectural change of the ADC, or architectural reconfigurability. These blocks can also be changed, for instance how the amplifiers are biased, or how many bits of resolution that a quantizer has in a SAR ADC.

3.1.1 Functional Block Diagram

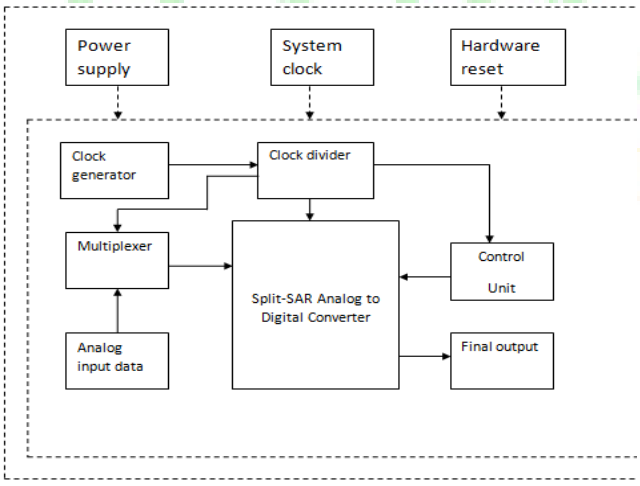

Fig. 5 Functional Diagram of Proposed System

3.1.2 Design Approach:

The design method includes clock controlled Configuration blocks are included, the design made as a user platform for different frequencies.

CLK	CLR	CONFIGURABLE INPUT	ANALOG VALUES	DIGITAL OUTPUT / RESOLUTION
1	1	000	0.001	0.024
1	0	001	0.024	0.070
1	0	010	0.047	0.116
1	0	011	0.070	0.162
1	0	100	0.093	0.185
1	0	101	0.116	0.208
1	0	110	0.136	0.254
1	1	111	0.162	0.024

TABLE 1: ANALYSIS TABLE

3.2 Module Design Flow:

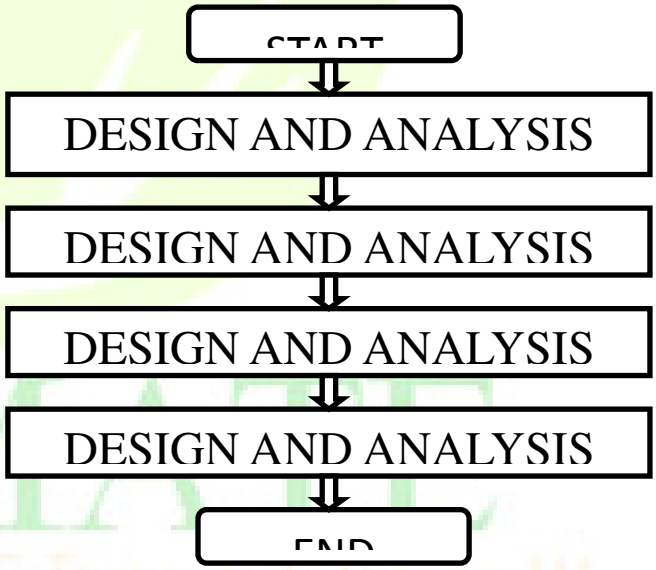

Fig.6 Flowchart Diagram for Design Process

3.2.1 MODULE DESCRIPTION:

In this first module we design the selective network for giving the appropriate input to the successive approximation registers ADC and analyse the performance of the designed network. In this second module we design the sample and hold circuit for processing the

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given analog signal from the selective network. Here after we measure the performance of the designed circuit.In this third module here design the successive approximation registers logic for effective analog to digital conversion in the SAR ADC.Finally integrating all the sub modules and output signals are routed into the required ports as per the FPGA device.

3.2.2 SONDAE_APPLICATION

Radiosonde:

A Radiosonde (Sonde is French and German for probe) is a piece of equipment used on weather balloons that measures various atmospheric parameters and transmits them to a fixed receiver. Radiosonde may operate at a radio frequency of 403 MHz or 1680 MHz and both types may be adjusted slightly higher or lower as required. A raw in sonde is a Radiosonde that is designed to only measure wind speed and direction. Colloquially, raw in sondes are usually referred to as Radiosonde.

Modern Radiosonde measure or calculate the following variables:

Pressure
Altitude
Temperature
Wind (both wind speed and wind direction)

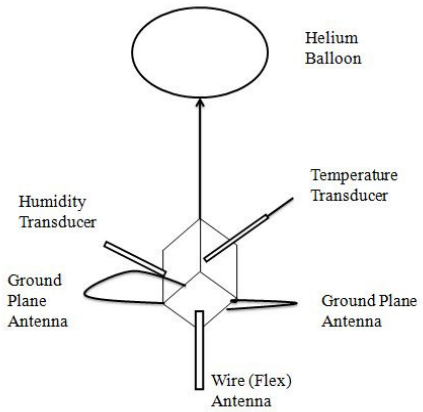

Fig.7RadiosondeMeasuring Ozone Concentration

There are two primary purposes of upper-air soundings: to analyse and describe current weather patterns and to provide inputs to short- and medium range computer-based weather forecast models. One very important, specialized use of atmospheric soundings is in support of forecasting hurricane movement. Special Radiosonde called drop wind sondes are launched from weather reconnaissance aircraft to observe atmospheric structure in the core of the hurricane as well as in the area downwind of the storm itself.

IV. EXPERIMENTAL RESULTS AND COMPARISON

4.1 ANALOG SIGNAL

The analog signal simulation result is shown in given figure 8 in this method, the input is clock(clk), clear(clr) and configurable input(config). First assign the analog signal and quantization value set to be real value. Same as the resolution value also set to be real.

Condition for an analog signal output:

If clr='1' then
cnt<="0000"
else if Rising_edge (clk) then
cnt<= cnt+1;

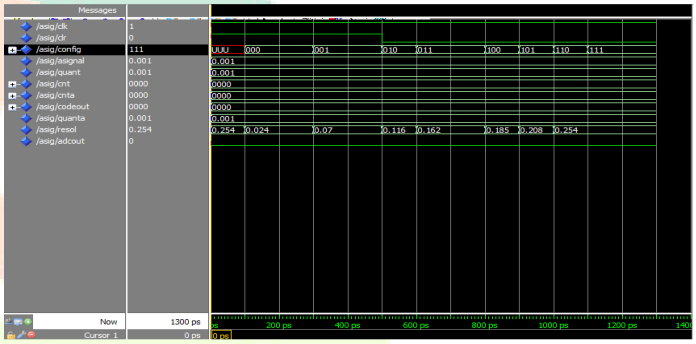

Fig. 8 Simulation Result for Analog Signal

4.2 INTEGRATION

Integration is the combination of all other units. This integration simulation resultis shown in given figure 9. This screenshot is shown the all other above function output is combined graph is shown. Here I mentioned the module step one by one.

- Module 1: asig port map (clk, clr, config)
- Module 2: sonde_application port map (clk, clr);

env_status<="**NORMAL**";
env_status<="**HOT**";
env_status<="**RAINY**";

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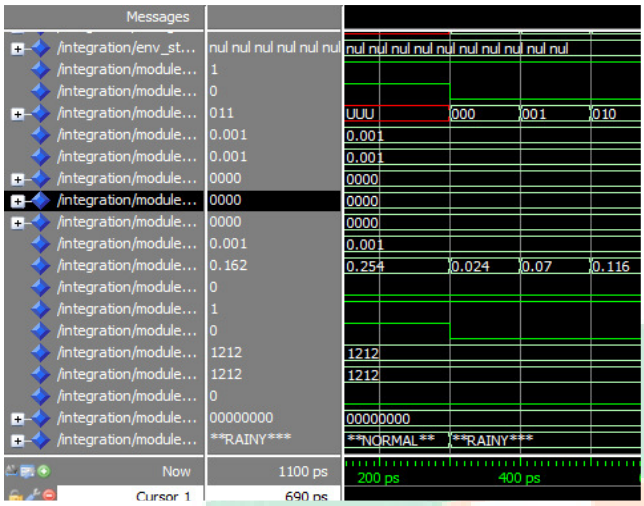

Fig.9 Simulation Results of Integration

VI. CONCLUSION

The SAR ADCs operating at tens of MS/s with conventional and V_{CM}-based switching were presented. The linearity behaviours of the DACs switching and structure were analysed and verified by both simulated and measured results. The V_{CM}-based switching technique provides superior conversion linearity when compared with the conventional method because of its array's capacitors correlation during each bit cycling. The reduction of the maximum ratio and sum of the total capacitance can lead to area savings and power efficiency which allow the SAR converter to work at high-speed while meeting a low power consumption requirement. The ADC achieves 1.46mW power consumption and occupies only 0.012mm2.The measured performance corresponds to an FOM of 39fJ/conversion-step, which is comparable with the best published ADCs.

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