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ADDITION AND SUBTRACTION USING LOGARITHMIC NUMBER SYSTEM FOR DIGITAL FILTERS

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ABSTRACT

In this project presents techniques for low-power addition & subtraction in the Logarithmic Number System (LNS) andquantifies their impact on digital filter VLSI implementation. The impact of partitioning the LUTrequired for LNSaddition & subtraction on complexity, performance, and power dissipation of the corresponding circuits is quantified. Two designparameters are exploited to minimize complexity, namely the LNS base and the organization of the LNS word. In addition, techniques for the low-power implementation of an LNS multiply-accumulate unit areinvestigated. The results are demonstrated by evaluating the power dissipation, complexity and performance of severalFIR filter configurations comprising one, two or four MAC units.

Keywords: Logarithmic Number System, Computer Arithmetic, Digital Filter, FIR.

I. INTRODUCTION

Data representation is an important parameter in thedesign of low-power processors since it affects boththe switching activity and hardware complexity. The Logarithmic Number System (LNS) has been investigated as an efficient way to represent data in special purpose VLSI processors, since it allows for simple arithmetic circuits under certain

conditions. In particular, LNSexploits the properties of the logarithm to reduce the basicarithmetic operations of multiplication, division, roots, andpowers to binary addition, subtraction, and right and leftshifts, respectively.

The dynamic range of floating point comes at the cost of lower precision and increased complexity over fixed point. Logarithmic number systems (LNS) provide a similar range and precision to floating point but may have some advantages in complexity over floating point for certain applications. This is because multiplication and division are simplified to fixed-point addition and subtraction, respectively, in LNS. However, floating point number systems have become a standard while LNS has only seen use in small niches.

II.BASICS OF LOGARITHMIC NUMBER SYSTEM

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The basic idea in LNS is to use logarithms to representdata. Since the logarithm of a negative number is not real,in order to represent signed numbers in LNS, the signinformation is stored as a separate bit a_x, and used incombination with the logarithm of the magnitude of thenumber. Furthermore, since the logarithm of zero is not afinite number, an additional single-bit flag z_X is used todenote that a number is zero. Summarizing, X denotes theoriginal number, x denotes the logarithm of the absolutevalue of |X|, and X_{LNS} is a triplet containing the signbit, the zero bit and x. Formally in LNS, a number X isrepresented as the triplet

$$X_{LNS} = (Z_x, S_x, Z)$$

Due to the basic properties of the logarithm, the multiplication of X_{LNS} and Y_{LNS} is reduced to the computationof the triplet Z_{LNS} ,

$$Z_{LNS} = (Z_z, S_z, Z)$$

Where, $z_Z = z_X \vee z_Y$,$s_Z = a x_{\oplus} s_Y$, and z = x + y.Similarly the case of division reduces to binary subtraction. The derivation of the logarithm a of the sum A of twotriplets is more involved, as it relies on the computation of

$$a=\max\{x, y\} + \log_b(1 + b^{-|x-y|})$$
$$= \max\{x, y\} + \varphi a\ (d),$$

where $\varphi_a\ (d) = \log_b\ (1 + b^{-d})$ and

$$d = |x - y|$$

Similarly the derivation of the difference of two numbers,requires the computation of

$$c=\max\{x, y\} + \log_b\ (1 - b^{-|x-y|})$$
$$= \max\{x, y\} + \varphi_s\ (d),$$

Where $\varphi s\ (d) = \log_b\ (1 - b^{-d})$. Assume that a two's-complement (TC) word is used to represent the logarithmx, composed of a k-bit integral part and an l-bit fractionalpart. The range DLNS spanned by x is given by

$$D_{LNS} = \left[-b^{2^{k-1}-2^{-l}}, -b^{2^{-l}}\right] U\{0\} U \left[b^{2^{-l}}, b^{2^{k-1}-2^{-l}}\right]$$

to be compared with the range of $(-2^{i-1}, 2^{i-1} - 2^{-f})$ of alinear TC representation of i integral bits and f fractionalbits. In general, LNS offers a superior range, over the lineartwo's-complement representation. This is achieved usingcomparable word lengths, by departing from the strategyof equispaced representable values and thus resorting to ascheme that resembles floating-point arithmetic. The basicorganization of an LNS adder &subtractor is shown in Fig.2.The parallel subtractions

$$s_1 = x - y$$
$$s_2 = y - x$$

are implemented, followed by a multiplexer, which computes d according to the rule

$$d = |x - y| = \begin{cases} s_1, & s_1 > 0 \\ s_2, & \text{otherwise} \end{cases}$$

III.PROPOSED DESIGN METHODOLOGY

This project presents a low-power design framework forLNS-based systems,

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composed of several techniques. Wequantify the impact of the constituent design techniquesusing detailed simulations of the derived LNS circuits.The proposed design framework is depicted in Fig.1.Initially, optimal selection of LNSdesign parameters is sought, including wordlength and baseassuming simple partitioned look-up table architecture.Subsequently, in the second stage of the proposed framework design techniques and the derived architectures arepresented, targeting LNS multiply-accumulate (MAC) unitsin 180nm technology. To illustrate the use of the proposed framework, the area-time-power design space of a low-pass FIR filter is explored for several configurations of MAC units. The proposed study focuses on the use of partitioning as a technique to limit the exponential growth of the size of LUTs with the wordlength. The technique is simple and leads to fast circuits.

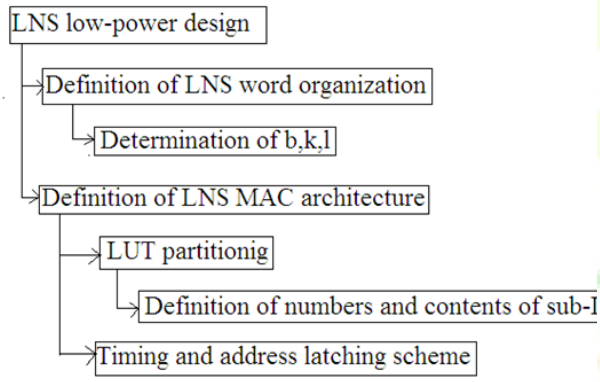

Fig.1. Proposed Design Methodology

Departing from direct look- up table organization, a variety of LNS architectures for addition, subtraction, and multi-operand operations, have been proposed in the literature employing interpolation, linear or polynomial approximation aiming at reducing the memory requirements, particularly for larger word lengths, such as 32 bits. These ideas have been combined with mathematical decompositions and transformations of the basic operations, exploiting the particular characteristics of the functions to further simplify approximation.

IV. LOW-POWER DESIGN OF LNS CIRCUITS

In the proposed design framework, power dissipationreduction is sought by partitioning the particular LUTsinto smaller LUTs, called sub-LUTs, only one of which isactive per operation. This organization is shown in Fig.4.2.To guarantee that no dynamic power is dissipated in theinactive sub-LUTs, the corresponding sub-LUT addressesare latched and remain constant throughout a particularoperation. Further power dissipation reduction is soughtat the implementation of multiply-accumulate units, byusing retiming techniques, as well as at the algorithmicoptimization level by judiciously selecting the parametersof the LNS representation.

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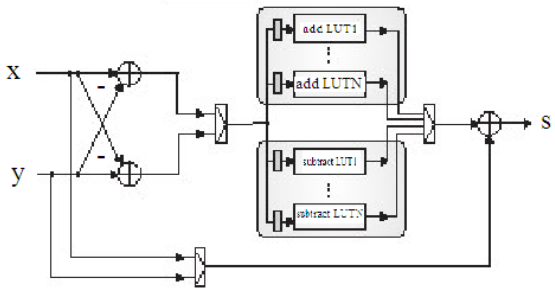

Fig.2. The organization of an LNS adder and subtractor

Complexity reduction in LNS processors by partitioningof the LUTs has been successfully applied in the past.Here we focus on combinational logic implementationof LUTs, instead of memory-based implementation. Theorganization of the LNS adder/subtractor comprises N sub-LUTs per operation, as shown in Fig.4.2. The upper sub-LUT system corresponds to function φ_a (d) required forLNS addition, i.e., addition of operands having the samesign, while the lower sub-LUT system is used for LNSsubtraction, i.e., addition of operands of different signs.

V. LNS MAC ARCHITECTURES

The basic structure of the single-MAC unit is shown inFig.3. Symbols and denote a multiplier and an adderrespectively, while D denotes a delay unit, implemented asa register. The study is extended to the performance of atwo-MAC and four MAC architecture, shown in Figs.4and Fig.5 respectively.

An FIR filter is described by,

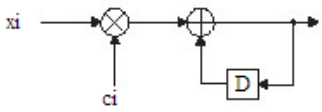

Fig.3. Organization of single MAC Architecture

$$y(n) = \sum_{j=0}^{N-1} C_i X(n-i)$$

Where C_i are the filter coefficients, X(n) is the inputsequence and Y(n) is the output sequence. In order to mapthe computation into two-MAC architecture, computation is partitioned into the computation of two terms,subsequently added, as follows

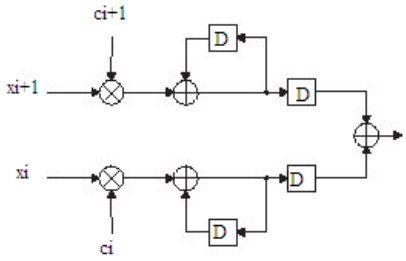

Fig.3. Organization of two MAC Architecture

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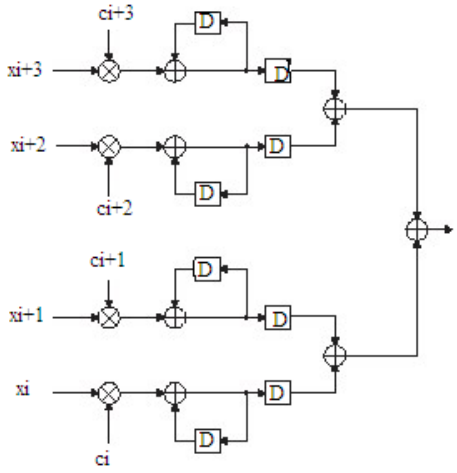

Fig.3. Organization of four MAC Architecture

$$y(n) = \sum_{j=0}^{\lfloor \frac{N}{P} \rfloor - 1} X(n-2j)C_{2j} + \sum_{j=0}^{\lfloor \frac{N}{2} \rfloor - 1} X(n-2j-1)C_{2j+1}$$

Each term is allocated to a MAC of two-MAC architecture. In general, for a P-MAC architecture, the computationis decomposed as

$$y(n) = \sum_{j=0}^{\lfloor \frac{N}{P} \rfloor - 1} X(n-Pj)C_{Pj} + \cdots + \sum_{j=0}^{\lfloor \frac{N}{P} \rfloor - 1} X(n-Pj-P-1)C_{Pj+P-1} = \sum_{p=0}^{p-1} \sum_{j=0}^{\lfloor \frac{N}{P} \rfloor - 1} X(n-Pj-p)C_{Pj+p}$$

The pth MAC unit computes Sp = X(n – P $_j$ –p)C$_{P\ j+p}$. Subsequently, the summation of all Sp is computed. The LNS equivalent of a single-MAC architectureis depicted in Fig.6, where the binary multiplier hasbeen replaced by an adder, and the binary adder is mappedto an LNS adder/subtractor.

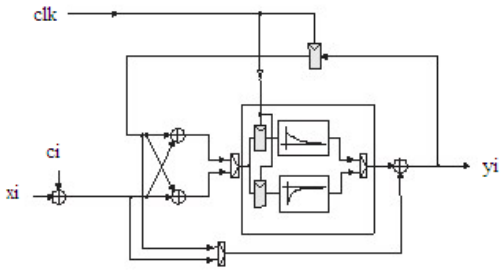

Fig.6.LNS MAC unit

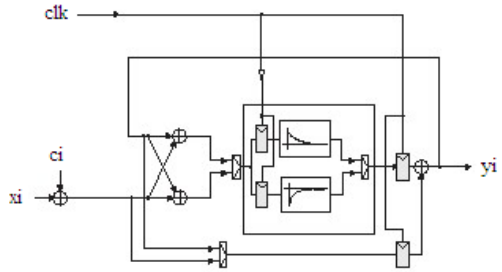

Fig.7. Retimed LNS MAC unit

In the implementation ofFig.6, it is evident that the paths to the inputs of the finaladder are not balanced, thus leading to excessive switchingactivity at the adder following the memory structure. Theamount of the switching activity depends on the logic depthof the LUT implementation. A solution to this problem is toretime the circuit so that the register located at the feedbackpath is replaced by registers placed at the inputs of the finaladder, as shown in Fig.7. Power dissipation simulations have shown that the retimed circuit is more efficient.Hence, the retimed circuit is adopted for the LNS MACimplementations.

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VI. RESULTS AND DISSCUSSION

The LNS adder &subtractor is simulated by using Cadence Tool as shown in Fig.8., X and Y inputs are added and subtracted with the X-Y and Y-X respectively. Addition or subtraction values are selected using MUX and the values are taken from the look-up table(LUT) and the waveform shows the output S.

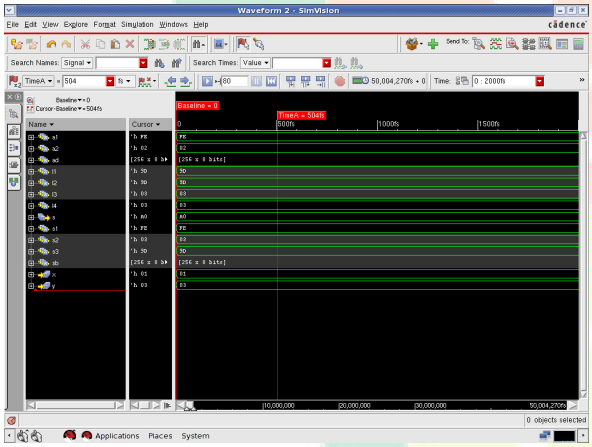

Fig.8. Simulation Result for LNS adder &subtractor using Cadence

The LNS MAC Architecture is simulated by using Cadence Tool as shown in Fig.9., the LNS is implemented using the MAC unit. X and Y inputs are added and subtracted with the X-Y and Y-X respectively. Addition or subtraction values are selected using MUX and the values are taken from the look-up table(LUT) and the waveform shows the output S.

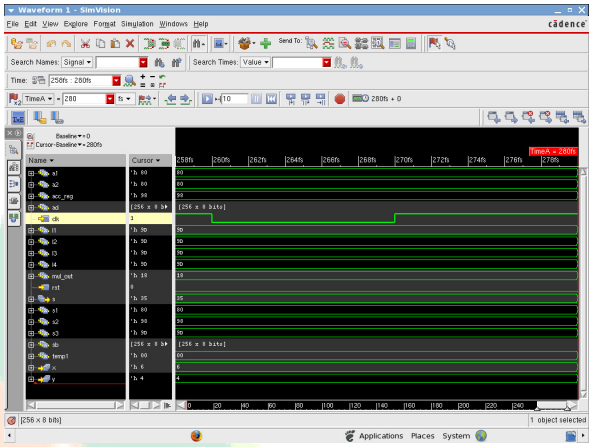

Fig.9. Simulation Result for LNS MAC Architecture using Cadence

VII.CONCLUSIONS

This project quantitatively shows that the adoption of LNScan lead to very efficient circuits for digital filtering applications when appropriately selecting the logarithmic base andthe wordlength in a contemporary 180nm technology. AnLNS-based system using the proposed adder &subtractors offers substantial power dissipation savings at no performancepenalty. Partitioning of the LUTs is employed to createparts in the circuit that can be independently activated thusreducing power dissipation. Power has been reduced bylatching the inputs to the LUTs.

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