ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com

International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2,Special Issue 6, March 2016

THERMAL ANALYSIS IN 3D IC FOR RANDOM HEAT FLUX

S.Suresh[1] , D.Tamilvendhan[2]
Assistant Professor[1,2], ECE, Sree Sastha Institute of Engineering and Technology,Chennai

Abstract: **Three-dimensional Integrated Circuits (3D IC) is a emerging technology in getting high performance IC's. To provide New Heat management technique in three dimensional stacked ICs, fluidic cooling scheme is processed and manipulated.The Analysis of cooling mode with normal mode on thermal management are scaled using Through Silicon Vias(TSV).The results leads to high internal pressureand pressure drop.Due to high energy carriers,Significant flow rate is processed.In general, a New cooling scheme with a dedicated approach to the High energy heat management could improve the cooling system performance.**

Index Terms : 3D IC,Random Heat Flux,Pressure Drop, Microfluidic Cooling

I. INTRODUCTION

As we are using large number of interconnects like Resistors, Capacitors & Delays in Complementary MOS Technology, the performance challenges are highly critical [1]. Interconnects are described as wires. For Giga scale Integrated Systems, wires are processed at ultra high speed, also increases the wire length [2]. The Power consumption in IC's leads to increasing wires and the process is used for distributing clock[3]. Unlike wafer to wafer routing, Chip to chip routing is used for enabling 3D IC stacking. 3D IC Provides maximum device density and minimize area of chips. Three Dimensional Integration could be used mainly on reducing length of wires and partitioning a chip into smaller ones.

To analyze and process three dimensional integrated circuits, issues relating thermal activities plays a vital role. Multiple layers of active devices are stacked and heat is dissipated. The interior layers of the three dimensional structure are thermally removed from the heat sink[7]. Heat transfer is further restricted by the low thermal conductivity bonding inter-faces and thermal obstacles in multiple IC layers.

Moreover, the inherent spatial non uniformity of the power and heat flux distribution/ dissipation within each active layer generates hot-spots of localized intense power dissipation, which yields a spot temperature increase, degrading the functionality of circuits and creating thermal stress issues due to non uniform thermal expansion. In particular, high temperatures brought by local hot-spots and/or excessive power consumption cause degradation of carrier mobility and escalated leakage power[8].

The design of thermal activity leads to sub-100 nm Integrated Circuits technologies has been one of the major challenges to the IC CAD group[9]. Spatially non uniform power distribution, have been substantially explored for planar 2D ICs. Thermal constraints using a processor-cache-memory system, and the performance of 3D architecture was compared with a conventional planar 2D design. This study considered for different device layers non uniformity of power distribution and resulting thermal couplings, but assumed a uniform power distribution within each layer.

However, in-plane non uniformity of power distribution and hot-spots will bring much higher local surface temperatures than predicted.Inter-layer cooling in vertically integrated high-performance chip stacks, in which several types of heat transfer structures have been explored.This paper proposed a cooling solution for 3D ICs, which features the use of new type of micro channel heat sink in each stratum of the 3D stack and the use of wafer-level batch fabricated electrical and fluidic chip input/output I/O interconnects. The routing with multifunctional interconnects, including through-silicon-vias TSVs for signal, thermal, and power distribution networks in 3D ICs and demonstrated the methodology to account for various physical space electrical and thermo mechanical requirements.

Thermal performance of the 3D circuit architectures remains a critical bottleneck, and further investigation of different cooling schemes and associated performance improvement is needed. In this work, the integrated interlayer micro fluidic cooling scheme is adopted and numerically investigated. Using the model, the effects of the cooling mode i.e., single-phase versus two-phase convective cooling and geometry variation on the cooling performance are quantitatively analyzed, yielding an insight and guidance on the TSV scaling and electrical interconnect congestion. The heat transfer and pressure drop performance of the two modes are evaluated and compared. Lastly, the significance of planar non uniformity of power distribution resulting in a presence of spatially distributed hot-spots is discussed.

II. THREE DIMENSIONAL STACKED INTEGRATED CIRCUITS FOR POWER MAPPING

The Figure shows the spatial heat flux distribution, or power map, of the 45 nm Intel Core 2 Duo processor code in which the two cores are mirror images of each other right below the L2 cache. To create this map, a publicly released die photo was examined and the floor plan was generated. The total power of each core and L2 cache are examined. The power density of L2 cache region is smaller than L1.

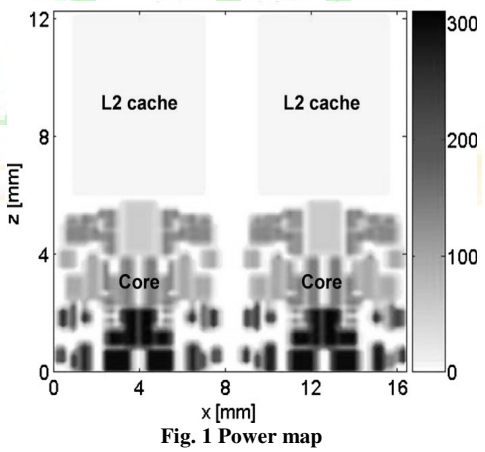


Fig. 1 Power map

ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2,Special Issue 6, March 2016

Micro fluidic channel layer capped with polymer cover are integrated for thermal management of each high-power processor tier. While the active layers are the main power consuming layers, heat is also generated in the metal-oxide layers due to Joule heating. The micro fluidic channels are capped with thin polymer coatings.

The thicknesses of the cover and the metal-oxide layers are set The dimensions are taken for the baseline channel depth, width, side-wall thickness, and base thickness. Unless specifically noted, all of the calculations reported have been conducted for the baseline geometry described. The physical dimensions of the micro fluidic Channels are parametrically varied within the ranges listed.

III MODEL DESCRIPTION

The thermal model is enhanced to deal with the three-dimensional thermal transport including the lateral temperature and fluid flow rate distribution due to non uniform power/heat flux distribution. The cross-sectional view of the 3D-stacked IC with embedded micro fluidic channels. It is assumed that the temperatures of the fluid and the solid domains including the side-wall base. The oxide layer is different but uniform at each cross section within each control.

$$x(di/dz) = \eta*h(i)*p(x) + h(i)*w(x) \text{ --------(1)}$$

Equation (1) represents the fluid enthalpy change due to the convective heat transfer owing to the temperature difference between the solid and fluid. The two terms on the right-hand-side of Eq. (1) does account for the vertical across the stack thermal coupling between the layers, which in essence specify the thermal Resistances between each fluid-filled channel in a given chip layer and the walls above and below it. Since these interlayer walls are Shared between the different layers in the stack, it provides thermal coupling between the layers and is equivalent to an interface condition between the layers that would be used in a more general 3D formulation of the problem.

Several correlations for two-phase heat transfer coefficients It has been proposed for small channels and/or micro channels.The boiling number allows one to determine the quality at which the transition from nucleate-boiling dominated to convective boiling dominated heat transfer occurs.The occurrence of nucleate boiling-dominated heat transfer could be attributed.

The heat transfer coefficient decreases as vapor quality increases, which suggests that nucleate boiling is the dominant heat transfer mechanism, regardless of vapor quality at these heat fluxes. For these conditions, the heat transfer coefficient is almost constant or slightly decreases, as the vapor quality increases. Therefore, an enhancement of heat transfer in two phase flow due to convection, which increases with increasing vapor quality, is largely suppressed so that the heat transfer coefficient is fairly independent of vapor quality change.

The model suggests that nucleate boiling is a dominant two phase heat transfer mechanism. The single-phase pressure drop along the micro fluidic channel. A fanning friction factor for laminar flow in a rectangular channel and equation for turbulent flow were adopted.

The single-phase pressure drop along the microfluidic channel is obtained from the fluid momentum balance Equation.A fanning friction factor for laminar flow in a rectangular channel and Blasius equation for turbulent flow were adopted according to the equations f_{lam} & $f_{tub.}$

For two-phase pressure drop, a separate model with a two-phase multiplier is used and proposed a correlation for the C value, which appeared in the classical twophase multiplier correlation.The void fraction can be calculated using the model of
de-ionized water is considered as a working fluid for single phase cooling.

For two-phase cooling, several refrigerants have been explored with their critical pressures and saturation pressure ranges corresponding to the temperatures range of 10–70°C. The resulting system of linear algebraic equations is iteratively solved using the successive under relaxation method. The thermophysical properties of water and the refrigerants are determined .The inlet fluid temperature for the single-phase cooling was set at 30°C at atmospheric pressure. For two-phase cooling, all the working fluids enter the microfluidic channels at saturated liquid state.

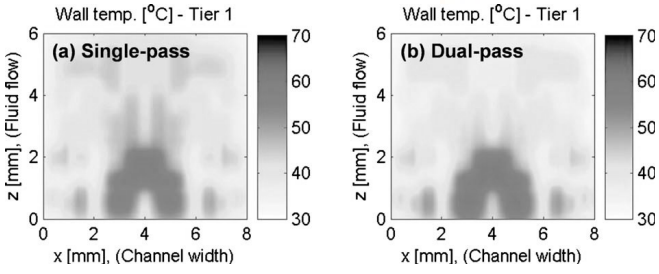
The corresponding saturation temperatures are set as 50°C for the refrigerants is required due to their small hydraulic budgets.Due to single inlet and exit ports for all microfluidic channels in the layer, the pressure drop from the inlet to the outlet of each microfluidic channel is fixed at 30 kPa and 50 kPa, for singlephase and two-phase cooling, respectively. Note that for twophase cooling with water as working fluid, fixed pressure drop of 20 kPa was imposed considering the saturation pressure of 31.2 kPa at 70°C. It is assumed that the inlet and outlet pressure headers do not affect the mass flow rate maldistribution.

IV RESULTS AND DISCUSSIONS

Model Validation: We conducted an experimental study on the single-phase and two-phase convective flow with single-channel and multichannel microstructures. The multichannel design consists of 2 cm-long 40 micro fluidic channels. Due to the lateral heat loss, as well as the size mismatch between the attached heater and the micro fluidic channel, the heat flux is non uniformly distributed.

Both the pressure drop changes with respect to power dissipation. The measured pressure drop was unexpectedly higher. The middle point and the outlet local wall temperatures in are also well predicted, whereas the inlet local wall temperatures were slightly under predicted. Their microstructures had significant heat loss up to half of percentage.

Dual-Pass Microfluidic Channel Heat Exchanger: This paper presented a novel micro channel heat exchanger for single-phase flow, which has a split-flow arrangement dual-pass. By providing dual-pass for refrigerant flow inside micro channels, both the flow length and the mass flux of each micro channel are reduced by half so that the pressure drop can be significantly roughly by one-fourth reduced.



ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2,Special Issue 6, March 2016

Fig. 2 Distributions of Temperature

However, the thermal performance of dual-pass micro fluidic channel, with single-phase flow, seems to be slightly inferior to that of single-pass micro fluidic channel, as observed in Fig 2.the total pressure drop through the channel was fixed.The wall temperature at the strongest hot-spot was slightly increased by adopting the dual-pass configuration. It should be, however, noted that most of the hotspots are located in the lower part of the power map so that most of the dissipated heat 91% of total power from the core was imposed on the bottom set of channels, whereas the top channels have been largely unutilized.

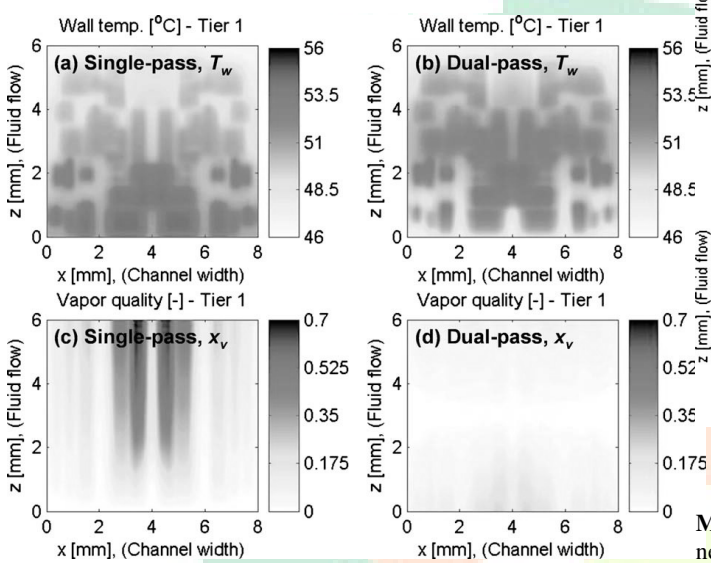


Fig. 3 Distributions of Vapour Quality

As expected, the mass flow rate due to the forementioned feature of dual-pass configuration, which made the thermal performance of the half length microfluidic channel comparable to that of full length microfluidic channel. For twophase flow, the dual-pass configuration featured slight improvement in hot-spot temperatures as observed in Fig 3.

Nonuniform Heat Flux : The total power generated from the nonuniform power map of all four tiers is 200 W. Assuming a uniform power dissipation map, with the same total power,yields the power density heat flux of 99 W/cm2 that would result in the highest wall temperature of _43°C.This means that the about 20°C of the wall temperature difference between the two simulated cases should be attributed to the in-plane nonuniformity of the power density, known as the hot spots.

The fluid temperature difference was around 5°C, which brought about a variation in the fluid properties, such as density and viscosity and, will be given a copyright form and the form should accompany your final submission.

Figure 4 shows that the micro fluidic channels in the hot-spot region have higher mass flow rates, which is consistent with the results.When the water temperature changes from 29°C to 34°C, both the viscosity and density decrease, but the density change is negligibly small. Thus, the reduced viscosity at the elevated fluid temperature should result in a smaller pressure drop.Under the fixed pressure drop condition, the viscosity reduction will reciprocally induce a higher flow rate through the microfluidic channels in the hot-spot region. This improves thermal performance of the single-phase microfluidic channel, and facilitates hot-spot temperature suppression because higher flow rate usually provides higher heat transfer coefficient.

Although the same power density and floor plan are imposed on each tier, vertical wall temperature differences and distribution are observed .This is because the first tier thermal management only depends on the microfluidic channel above it, while the other tiers have double-sided cooling,

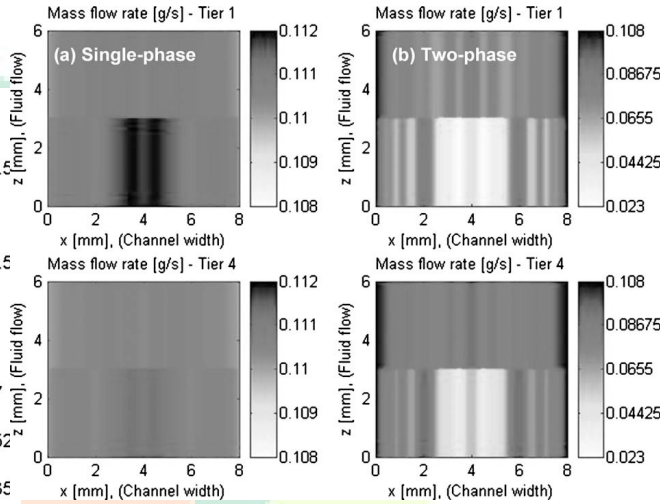


Fig. 4 Distributions of Mass Flow rate

Microfluidic Channel Geometry : The on-chip thermofluidic network is composed of fluidic TSVs and microfluidic channels. It is assumed that all the fluidic TSVs are located outside the region where all the gates and metal wiring are distributed.Thus, only microfluidic channels are considered for routing requirement analysis. Since microfluidic channels are fabricated on the back side of a silicon die, they do not affect routing capability on metal layers. However, these channels obstruct TSV connections.Due to their large size, the microfluidic channels decrease the routing capacity of TSVs quite considerably.
In fact, the scarcest resource is usually the signal TSV capacity. Due to the microfluidic channels placement, many routing tiles have no capacity left for signal TSVs.Therefore, the microfluidic cooling channels compete with wire routability for space.

Two-Phase Cooling.: For the baseline channel geometry,the calculated heat transfer coefficients for single-phase cooling were quite uniform,while two-phase heat transfer coefficients ranged from 5 to 7 with the average value of 3.5 using working fluid. If 10°C of driving temperature difference is taken, the two-phase cooling can, roughly, deal with the power density of 350 W/cm2, whereas a single-phase cooling capability is limited to 50 W/cm2. Moreover, single-phase flow has an additional penalty due to coolant temperature increase along the channel caused by the sensible heat transfer.
The inlet fluid temperature, therefore, should be much lower in a single phase flow, which requires larger cooling load at the air-side heat exchanger _or condenser_ in the system. Thus, the higher heat transfer coefficient and a relatively constant fluid temperature indicate a better thermal performance of a two-phase cooling system.

ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2,Special Issue 6, March 2016

V CONCLUSION

In the present study, we have numerically investigated the performance of interlayer microfluidic channel cooling for 3D stacked ICs. Both in-plane, as well as, vertical nonuniformity in heat flux for both single-phase and two-phase flow are examined. It is verified that the dual-pass heat exchanger greatly helps in augmenting the mass flow rate through microfluidic channels so that the outlet vapor quality can be reduced, and the reliability of the cooling system can be considerably enhanced in two-phase cooling.

Parametric investigation showed that increases of channel depth and channel base thickness are useful in reducing the wall temperature. However, this is limited by the maximum length scale of TSVs. The effect of channel width change was found not to be significant. For improved thermal performance, it is better to keep the channel side-wall thickness small; however, wider spacing between channels offers more vertical direction routing capacity.

A two-phase cooling scheme provided enhanced thermal performance as compared with single-phase cooling due to the higher heat transfer coefficient and relatively constant fluid temperature.Thermal performance of the two-phase water cooling was significantly degraded because of its poor hydraulic properties. In two-phase microfluidic channel cooling, pressure drop acted as the significant limiting factor. The reduced pressure can be a good indicator of refrigerant compatibility to two-phase microfluidic channel cooling. Mass flow rate maldistribution has been also observed.Due to the positive feedback between the mass flow rate reduction and a vapor quality increase, fluid flow avoids the channels passing through the hot-spot regions.

In summary, working fluids for two-phase cooling system, which performed satisfactorily in terms of reliability and showed superior performance to the single-phase cooling system.In general, however, dedicated hot-spot thermal management and the hybrid cooling schemes combining different cooling methods based on their power dissipation capability are expected to be the major drivers to improve the 3D IC cooling system performance by suppressing the mass flow rate distribution, maintaining temperature uniformity within the stack, and enhancing the reliability.

References

[1] Bohr, M. T., 1995, "Interconnect Scaling—The Real Limiter to High Perfor-mance ULSI," Tech. Dig. - Int. Electron Devices Meet., **1995**.

[2]Yamashita, K., and Odanaka, S., 1997, "Interconnect Scaling Scenario Using a Chip Level Interconnect Model," VLSI Technology Symposium.

[3] Banerjee, K., Souri, S. J., Kapur, P., and Saraswat, K. C., 2001, "3-D ICs: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration," Proc. IEEE, **89.**

[4] Semiconductor Industry Association, 2006, "The International Technology Roadmap for Semiconductors ITRS."

[5] Rahman, A., and Reif, R., 2000, "System-Level Performance Evaluation of Three-Dimensional Integrated Circuits," IEEE Trans. Very Large Scale Integr. VLSI Syst.,

[6] Lee, Y.-J., Kim, Y. J., Huang, G., Bakir, M., Joshi, Y., Fedorov, A., and Lim,S. K., 2009, "Co-Design of Signal, Power, and Thermal Distribution Networks for 3D ICs," *Proceedings Design, Automation and Test in Europe*, Nice,France.

[7] Im, S., and Banerjee, K., 2000, "Full Chip Thermal Analysis of Planar 2D and Vertically Integrated _3-D_ High Performance ICs," Tech. Dig. - Int. Electron Devices Meet., **2000**.

[8] Huang, W., Ghosh, S., Velusamy, S., Sankaranarayanan, K., Skadron, K., and Stan, M. R., 2006, "HotSpot: A Compact Thermal Modeling Methodology for Early-Stage VLSI Design," IEEE Trans. Very Large Scale Integr. _VLSI_ Syst.,**14**.

[9] Huang, W., Stan, M. R., Skadron, K., Sankaranarayanan, K., Ghosh, S., and Velusamy, S., 2004, "Compact Thermal Modelling for Temperature-Aware Design,"Design Automation Conference, San Diego, CA.

[10]Kirchheim, R., "Stress and Electromigration in Al-lines of Integrated Circuits," *Acta metall. Mater.* Vol. 40, No. 2 (1992).

[11] Ney, D., Federspiel, X., Girault, V., Thomas, O. and Gergaud, P., "Stress-Induced Electromigration Backflow Effect in Copper Interconnects," *IEEE Trans. Dev. Mater. Reliab.*, Vol. 6, No. 2 (2006).

[12] de Orio, R.L., Ceric, H. and Selberherr S., "Physically based models of electromigration: From Black's equation to modern TCAD models," *Microelectron. Reliab.*, Vol. 50, Issue 6 (2010)

[13] Ceric, H., de Orio, R.L., Cervenka, J. and Selberherr, S., "A Comprehensive TCAD Approach for Assessing Electromigration Reliability of Modern Interconnects," *IEEE Trans. Device. Mater. Reliab.*, Vol. 9, No. 1 (2009),

[14] Lienig, J., Jerke, G., "Electromigration-Aware Physical Design of Integrated Circuits*," Proc 18th Inter. Conf. VLSI Design*, Kolkata, India, Jan. 2005.

[15]Lu, K., Pan, D.Z., "Reliability-aware Global Routing under Thermal Considerations," *Proc 1st Symp. Quality Electronic Design Asia*, Kuala Lumpur, Malaysia, July 2009.

[16] Black, J.R., "Mass Transport of Aluminum By Momentum Exchange with Conducting Electrons," *Proc 6th Reliab. Phy. Symp.*, Los Angeles, CA, Nov. 1967, pp. 148-159.