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# Design and Analysis of Digital Circuits Using QCA Logic

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***Abstract*— In this paper the area and complexity are the major issues in the circuit design.QCA are a promising, emerging nano-technology based on single electron effects in quantum dots and molecules. Such devices exhibit a small-feature size, high clock frequency and ultra low power consumption. QCA provides an alternative way of computing in which the logic states ("0" & "1") are defined by the position of electrons. Efficient solution has recently been proposed for several arithmetic circuits such as adders, multipliers and comparators. The design of binary comparator based on QCA is represented which employs the existing QCA majority gates for implementing the binary comparator. This paper proposes new design approach oriented to the implementation of full adders in QCA majority gates. In this design we try to reduce the optimization parameters like complexity,area and power consumption.The proposed design compared with previous one in terms of complexity (number majority gates used), speed, area and power consumption this gives the proposed design of comparator in QCA is more efficient than the prior design.**

***Keywords*— QCA, MG, Quantum dot**

## I.INTRODUCTION

In vlsi design power, speed and area are the most often used measures for determining the performance of the vlsi design. Rapid growth in internet and mobile technology, exchange of information is common practice. Information may be text, audio, video etc form. Transmission of information through a physical medium or wireless medium, possibility that data get corrupted this leads to an error in a random only selected locations of a symbol or the entire symbol. To have a reliable communication through a communication channel that has an acceptable bit error rate(BER) and high signal to noise ratio(snr) error correcting codes are used. These codes are used to detect and correct a specific number of error which may occur during transmission of message over a communication channel.

There are different types of error correction codes are used in present digital communication system based on the type of channel noise.Few of them are hamming code,low density parity check code (ldpc),Bose chaudhuri hocquenghem code (bch),Reed Solomon code (rsc), and Turbo code(tc).these codes are different from each other in their complexity and implementation.bch codes are widely used in the area like,mobile communication, digital communication, satellite communication ,optical and magnetic storage system and computer network etc.

In this work(15,7)bch encoder and decoder is implemented on spartan 3e FPGA.for designing the bch codes, two coding techniques are used .they are systematic codes and non systematic codes. In case of systematic codes original message d(x) is as it is in the encoded word c(x).where as in case of non –systematic code encoded word c(x) is obtained by multiplying message d(x) with generator polynomial g(x).hence message data will not be same in the encoded code word .

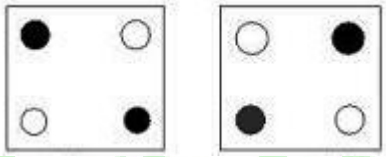
The electronics industry has achieved a phenomenal growth over the last two decades mainly due to the rapid advances in integration technologies; Large-Scale systems design in short, due to the advent of VLSI. The number of applications of integrated circuits in high-performance computing telecommunications and consumer electronics has been rising steadily and at a very fast pace. It is mainly based on the transitior leve packaging and the number of interconnections in a single chip.Typically the required computational power of these applications is the driving force for the fast development of this field. One of the most

important characteristics of information services is their increasing need for very high processing power and bandwidth. The other important characteristics is that the information services tend to become more and more personalized which means that the devices must be more intelligent to answer individual demands and at the same time they must be portable to allow more flexibility and mobility

## II.QUANTUM DOT CELLULAR AUTOMATTA

Quantum Cellular Automata (QCA) is a nanotechnology that has recently been recognized as one of the top six emerging technologies with potential applications in future computers. It has gained significant popularity in recent years. This is mainly due to rising interest in creating computing devices and implementing any logical function with that. The basic building block of QCA circuit is majority gate; hence, efficiently constructing QCA circuits using majority gates. Several studies have reported that QCA can be used to design general purpose computational and memory circuits. QCA is expected to achieve high device density, very high clock frequency and extremely low power consumption.

In recent years the development of integrated circuits has been essentially based on scaling down that is, increasing the element density on the wafer. Scaling down of complementary metal oxide semiconductor CMOS circuits, however, has its limits. Above a certain element density various physical phenomena, including quantum effects, conspire to make transistor operation difficult if not impossible. If a new technology is to be created for devices of nanometer scale, new design principles are necessary. One promising approach is to move to a transistor less cellular architecture based on interacting quantum dots, figure-1 shows quantum dot cellular automata QCA.



a.logic '0' b. logic '1'

Figure-1 QCA Cell

## II.RELATED WORKS

In author[1] Multiple-valued logic can be used to decrease the average power required for level transitions and reduces the number of required interconnections, hence also reducing the impact of interconnections on overall energy consumption. The proposed implementation overcomes several limitations found in previous quaternary implementations published so far, such as the need for special features in the CMOS process or power-hungry current-mode cells. We present a full adder prototype based on the designed LUT, fabricated in a standard 130-nm CMOS technology, able to work at 100 MHz while consuming 122 $\mu$W[1].

It has two types Quaternary and ternary logic. In existing system Quaternary logic LUT is used to design the Multiplexer[1]. In author[2] The area and complexity are the major issues in circuit design. Here, we propose different types of adder designs based on Quantum dot Cellular Automata (QCA) that reduces number of QCA cells and area compare to previous designs. The quantum dot cellular automata is a novel computing paradigm in nanotechnology that can implement digital circuits with faster speed, smaller size and low power consumption. By taking the advantages of QCA we are able to design interesting computational architectures. The QCA cell is a basic building block of nanotechnology that can be used to make gates, wires and memories. The basic logic circuits used in this technology are the inverter and the Majority Gate (MG)[2]. using this other logical circuits can be designed. the adders such as half, full and serial bit were designed and analyzed. These structures were design with minimum number of cells by using cell minimization techniques The proposed method can be used to minimize area and complexity. These circuits were designed by majority gate and implemented by QCA cells[2]. In author[3] The Quantum-dot Cellular Automata (QCA) approach represents one of the possible solutions in overcoming this physical limit. In the existing method, a Quantum-dot Cellular Automata adder is designed using three input Majority Gate (MG). This Ripple Carry adder (64-bit) spans over a complexity of 16667 (cell count) covering 18.72 $\mu m^2$ of active area and shows a delay of 9 clock cycles, that is 36 clock phases. In proposed method the same 3-input Majority logic gate method for constructing QCA is applied. But in the modified adder (64-bit) layout design outperforms all state-of-the art competitors and reduces area-delay efficiently than previous designs. The modified QCA Ripple Carry adder designed spans over a complexity of 15939 (cell count) covering 15.32 $\mu m^2$ of active area and shows a delay of only $8\frac{1}{4}$ clock cycles, that is just 33 clock phases. Here the cell count is reduced by 7% when compared to existing design[3].In author[4] to implement a novel XOR gate. The gate is simple in structure and powerful in terms of implementing digital circuits.By applying the XOR gate, the hardware requirement for a QCA circuit can be decrease and circuits can be simpler in level, clock phase and cell count. In order to verify the functionality of the proposed device some implementation of Half Adder (HA) and Full Adder (FA) is checked by means of computer simulations using QCA-Designer[4].

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## III.PROPOSED MODEL

The proposed model of this system(QCA) has overcome the disadvantages of the works which is given above. it is also used to design the Various sequential and combinational circuits. hence Majority gates are used to design the comparator circuit it is an emerging nanotechnology, with the potential for faster speed, smaller size, and lower power consumption than transistor-based technology. This QCA gates have two types MG and MV and etc., MG means Majority gate and MV means Majority voter. QCA cell is constructed from four quantum dots arranged in a square pattern in shown in the .These quantum dots are sites electrons can occupy by tunneling to them. The proposed model of QCA based majority gate comparator shown in the Figure-2

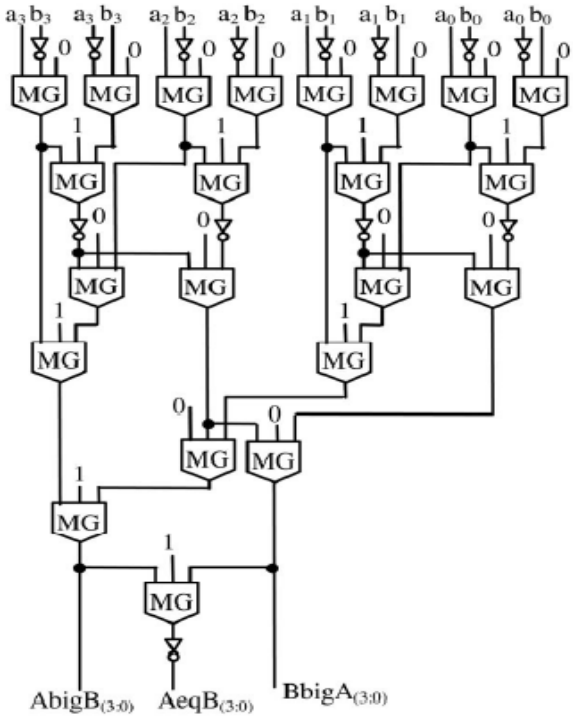


Figure-2 Conventional 4 bit majority gate comparator(using QCA logic)

## IV.QCA MAJORITY LOGIC GATE

Majority gate-based logic is not normally explored with standard CMOS technologies, primarily because of the hardware inefficiencies in creating majority gates. As a result not much effort has been made towards the optimization of circuits based on majority gates. We are exploring one particular emerging technology, quantum-dot cellular automata (QCA), in which the majority gate is the fundamental logic primitive. One of its main applications is a simple and intuitive method for reduction of three-variable Boolean functions into a simplified majority representation. The method is based on Karnaugh maps (K-maps), used for the simplification of Boolean functions. the 3-input majority gate forms the fundamental logic primitive. Majority logic is a way of implementing digital operations based on the principles of majority decision. The logic element a majority gate has an odd number of binary inputs and a binary output. The output is a logical 1 when the majority of inputs is logic 1 and logical 0 when majority of inputs is logic 0.Any digital function can be implemented by a combination of majority gates and binary inverters. Majority logic provides a concise implementation of most digital functions encountered in logic-design applications. Figure -3 shows the basic majority gate

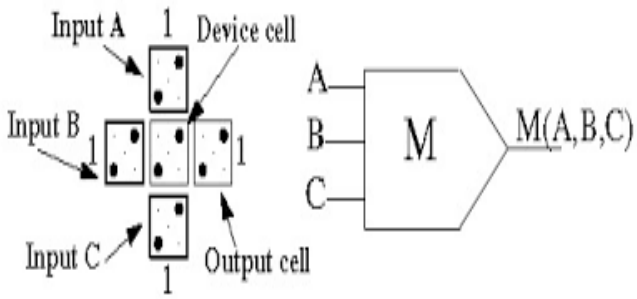


Figure-3 Majority Gate

The fundamental logic primitive that can be created with QCA is a majority gate or majority voter. In QCA, majority voter is the most fundamental gate. Majority gate in CMOS would consist of several transistors.

## V.OPERATION

Comparator is one of the important components in logic design. In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number. So comparator is used for this purpose. For example: Magnitude comparator is a combinational circuit that compares two numbers,A and B, and determines their relative magnitudes. The outcome of comparison is specified by three binary variables that indicate whether A>B, A=B, or A<B. Comparators are used in central processing units (CPUs) and microcontrollers.

The majority gate comparator is based on the AND and OR operation which includes both operation and it also includes the NOT gate function it works in the logic majority of inputs as the output.it will get the output as the three combinations.

A 1-bit binary comparator receives two bits a and b as inputs and establishes whether they are equal, less than or greater than each other. These possible states are represented through three output signals, here named AeqB, AbigB,BbigA, that are asserted, respectively, when a= b, a>b, and a<b.the conventional 4 bit magnitude comparator is designed and the conventional 4 bit majority gate comparator is designed based on the QCA logic to determine the area and delay compared to both and it is simulated by using Xilinx it works in the basic operation of basic gates which is used in the majority gate .it is also designed with the QCA designer.based on the given logic and the gates.basic two bit comparator is shown in figure-4 given below.

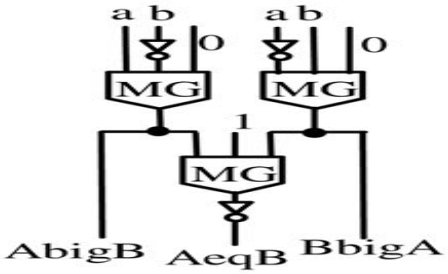


Figure-4 Two bit MG Comparator

With QCA, majority voter can be used in constructing AND and OR gates. This majority gate can be converted to either an AND gate or an OR gate by fixing one of the inputs to be permanently "0"or "1" respectively. Assuming the inputs are A, B and C, the logic function of a majority gate is shown below:

$$M(A, B, C) = AB+BC+AC$$

QCA circuit is based on majority gate-based circuits instead of AND/OR/Inverter gate-based circuits.

$$M(A, B, 0) = AB$$

$$M(A, B, 1) = A+B$$

## IV.ADVANTAGES AND APPLICATIONS

An emerging computational nanotechnology called QCA has been a great help in learning more about the majority gates, as it happens to be its primary logic primitive. Characterizing the three variable Boolean function to a simplifying majority illustration using the Karnaugh maps (K-maps) is one of the easiest application of majority gates.

The QCA cell has four quantum dots arranged in a square pattern. The fundamental logic primitive includes three inputs majority gate. Majority logic helps in the implementation of digital operations based on the principles of majority decisions. The logic elements a majority gate has an odd number of binary inputs and binary output. The output is a logical 1 when the majority of input is logic 1 and logical 0 when the majority of input is logic 0.The majority gates along with the binary inverters helps in the implementation of digital functions as per the logic design applications.

## V. RESULTS AND DISCUSSION

We have designed a magnitude comparator and calculated the area, delay . This is compared with the existing model .From our comparisons we achieved better performance based on the above mentioned criteria, it is shown in the below table-1 And the output of both comparators is simulated in Xilinx and model simulator and implement by using FPGA.

| Parameters | Conventional 4 bit magnitude comparator | Conventional 4 bit majority gate comparator(using QCA logic) |
|---|---|---|
| Delay | 8.805ns | 6.209ns |
| Area | 6% | 2% |

Table-1

Thus the comparison chart for the comparators is given in the below figure-5 and figure-6.

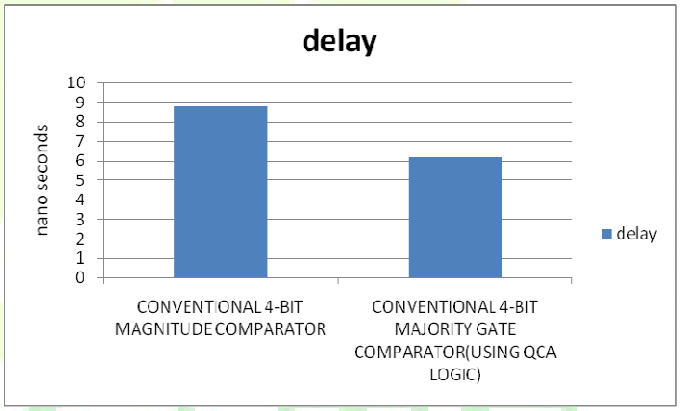


Figure-5 Delay comparison

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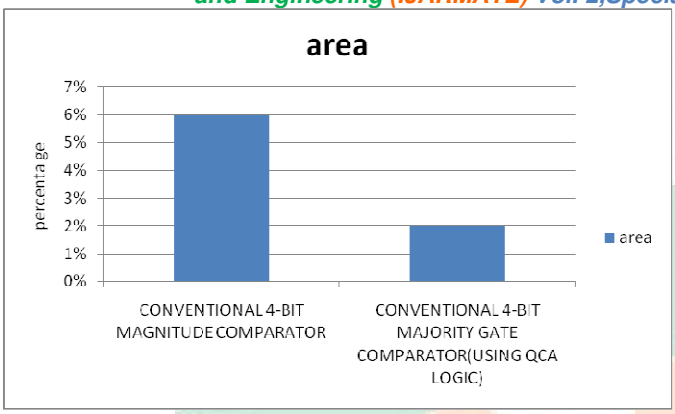


Figure-6 Area Comparison

## VI.CONCLUSION AND FUTURE WORK

Already we have designed the full adder in QCA using the basic QCA logic devices. Also we can design both combinational and sequential circuits using the QCA logic primitives such as majority gates, majority voters and inverter. Further, we can able to design the same circuit with QCA reversible logic gates for minimizing the garbage outputs as well as detection of faults in multi-bit error at the outputs. The major goal of reversible logic design and synthesis is to minimize the garbage outputs and the quantum cost. Reversible logic has extensive applications in nanotechnologies such as quantum computing, QCA and optical computing. Thus, we can able to emphasize very special characteristics of the proposed approach of concurrent testing based on reversible logic for QCA computing. Hence, by cascading a reversible logic gate along with its inverse will result in dissipation less QCA circuits, as all inputs are regenerated for concurrent error detection of multi-bit error at the outputs that results in no information loss. In future, we can design the 1-bit reversible full adder for fault detection in QCA emerging nanotechnology implemented using the reversible logic gates

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