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Performance Analysis of Error Detection and Correction Using LDPC Codes

S V Sathyah
Assistant professor
Department of Electronics and Communication
TJS Engineering College
Peruvoyal , India
sv.sathyah@yahoo.com

P Komaleeswari
PG Scholar
Department of Electronics and Communication
TJS Engineering College
Peruvoyal , India
Komaleeswari.ece@gmail.com

ABSTRACT— **The complexity of communications and signal processing systems increases, so does the number of blocks or elements that they have typical example of those elements are digital filters. The increase in complexity also poses reliability challenges and creates the need for fault-tolerant implementations. In this proposed a scheme based on error correction coding has been recently proposed to LDPC code. In that scheme, each filter is treated as a bit, and redundant filters that act as parity check bits are introduced to detect and correct errors. The proposed scheme is first described and then illustrated with two case studies. Finally, both the effectiveness in protecting against errors and the cost are evaluated for a field-programmable gate array implementation. LDPC codes are used to design the encoder and decoder to reduce faults or error detection and correction in the channel. The errors can affect the arrangement of the input and it will create the problem in between the communication systems. The LDPC codes can detect and correct the errors and it will use the filters for the error correction. The channel is main unit in the communication unit and the error can be induced in that.**

Keywords— ***low density parity check codes, field programmable gate array***

I. INTRODUCTION

The basic goal in channel coding is to design encoder-decoder pairs that allow reliable communication over noisy channels at information rates close to capacity. The primary obstacle in the quest for practical capacity-achieving codes has been decoding complexity[1]. Low-density parity-check (LDPC) codes have, however, emerged as a class of codes that have performance at or near the Shannon limit and yet are sufficiently structured as to have decoders with circuit implementations. In addition to decoder complexity, decoder reliability may also limit practical channel coding. In Shannon's schematic diagram of a general communication system and in the traditional information and communication theories that have developed within the confines of that diagram, noise is localized in the communication channel. The decoder is assumed to operate without error. Given the possibility of unreliable computation on faulty hardware, there is value in studying error-prone decoding. In fact Hamming's original development of parity check codes was motivated by applications in computing rather than in communication[1]. A first step in understanding these issues is to analyze a particular class of codes and decoding techniques: iterative message- passing decoding algorithms for LDPC codes. Correspondence between the factor graph and the algorithm is not only a tool for exposition but also the way decoders are implemented [2] . In traditional performance analysis, the decoders are assumed to work without error. In this paper, there will be transient local computation and message-passing errors, whether the decoder is analog or digital

II. PREVIOUS MODELS

There are several algorithms which are used previously in communication systems to perform the error detections and correction. They are as follows:

a) Errors are fault tolerance in discrete-time dynamic systems, such as finite-state controllers or computer simulations, with focus on the use of coding techniques

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to ef- ficiently provide fault tolerance to linear finite-state machines (LFSMs)[2].

b) In nanometric technologies, circuits are increasingly sensitive to various kinds of perturbations. Soft errors, a concern for space applications in the past, became a reliability issue at ground level. Alpha particles and atmospheric neutrons induce single-event upsets (SEU), affecting memory cells, latches, and flip-flops, and single-event transients (SET), initiated in the combi- national logic and captured by the latches and flip-flops associated to the outputs of this logic[3]. To face this challenge, a designer must dispose a variety of soft error mitigation schemes adapted to various circuit structures, design architectures, and design con- straints[3].

c) efficient technique for implemen- tation of soft-error- tolerant finite impulse response (FIR) filters is presented. The proposed technique uses two implementations of the basic filter with different structures operating in parallel. A soft error occurring in either filter causes the outputs of the filters to differ, or mismatch, for at least one sample. The filters are specifically designed so that, when a soft error occurs, they produce distinct error patterns at the filter output. An error detection circuit monitors the basic filter outputs and identifies any mismatches[4].

d) channel model suitable in certain applications, namely the multi-input multi-output (MIMO) dele- tion channel. This channel models the scenarios where multiple transmitters and receivers suffering from synchronization errors are employed[5]. We then consider a coding scheme over such channels based on a serial concatenation of a low-density parity check (LDPC) code, a marker code and a layered space-time code[5].

III. LOW DENSITY PARITY CHECK CODES

Low-density parity check (LDPC) code, which was first presented by Gallaher in 1962 but only became popular when Mackay rediscovered it in 1995. It has been shown that with iterative soft-decision decoding LDPC codes can perform as well as or even better than turbo codes[6] . It is claimed that LDPC codes will be chosen in future standards, such as 4G, later versions of WiMax and magnetic storage devices.

A low-density parity check (LDPC) code is characterized by its sparse parity check matrix, that is a matrix containing mostly zero elements and few nonzero elements. Three important parameters are its code word length, n, its dimension, k, and its number of parity bits, $m = n - k$. The number of nonzero elements in a row of the parity check matrix is called the row weight, denoted by ρ. The number of nonzero elements in a column of the parity check matrix is called the column weight denoted by γ [1].

The G and H matrix obey the following rule: GHT = 0 Where T is the transpose operation. The G matrix consists of n rows and K columns. Just take your message bits (K bit length) and simply multiply with the G matrix. This operation gives you n-bit codeword. If you have a streaming array of message bits , divide your message into blocks of k bits length and do the multiplication with the G matrix repeatedly till your input bits are exhausted.

After you receive the code words, to check for errors, simply multiply the code words(n bits length) with H matrix. The H matrix contains n rows and n-K columns. This multiplication gives the bit position of the bit that is corrupted[6].

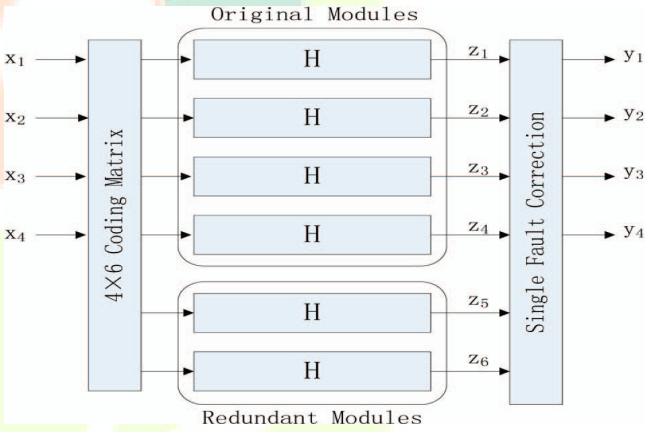

Fig.1. LDPC encoder and [1] .

IV. PROPOSED SYSTEM

First, let us discuss the decoding schedule. Fig. 1 illustrates the decoding flow for a simple universal-LDPC code. The schedule can be simply applied to other cases with different P, c, and t parameters. P columns are processed concurrently in one clock cycle. The left-most P columns are processed first, then the second left-most P columns, and so on. The column process and the row process are interleaved. In every clock cycle, VPUs get M check-to-variable messages and compute the M variable-to check messages, so that MPUs get one message each, so each MPU can deal with one step of the check node process. The whole check node process is divided into t steps. With this decoding schedule, we can finish one iteration in clock cycles. It is normally much faster than the traditional partly parallel decoder architectures.

The overall decoder block diagram is shown in Fig. 4.

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The critical part of this implementation is the network connecting VPUs and MPUs. The shuffle network transmits variable-to check messages. In the LDPC decoding algorithm, MPUs only communicate with VPUs and the row processes of different check nodes are independent of each other. In our Universal-LDPC decoder architecture, one block called MPU communication network is added to the MPUs to reduce the complexity of the shuffle networks.

Through the introduction of the MPU communication network, we can ensure that each MPU processes the variable-to- check messages from and transmit the check- to-variable messages to a fixed VPU during the entire decoding process. This will be illustrated more clearly later. In fact, the shuffle network connecting MPU sand VPUs only consists of M*b wires, where we assume each Messages iteratively exchange between VPU and MPU through the shuffle network. Data flow of row process intermediate result. message is quantized as b bits. Normally the quantization bits b is chosen as explains why each MPU always computes with the messages from a fixed VPU during the entire decoding process. With the simple shuffle network, MPU is connected with VPU X. The row process of each check node is separated into steps with one variable-to-check message being processed in each step. At the first clock cycle of an Messages iteratively exchange between VPU and MPU through the shuffle network iteration, having received the message from VPU X, MPU performs the first step of the row process.

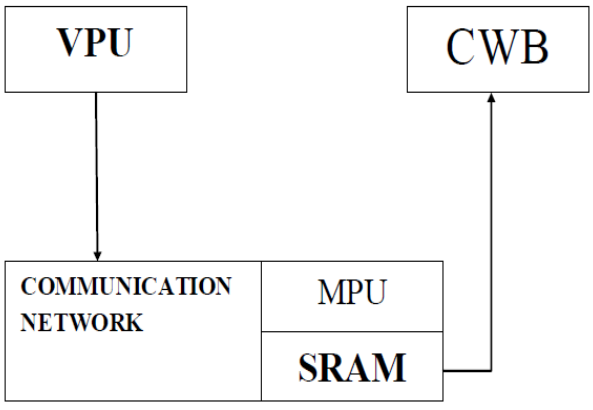

Fig.2. LDP DECODER In the figure 2, communication system connect to the VPU and MPU VPU means virtual private unit MPU means message processing unit .

V.IMPLEMENTATION OF PROPOSED SYSTEM

First of all, we show the message memory management in Fig. 3.We only save the row process results. In addition, the results are saved in a compressed way that only the minimum magnitude Shows the memory processor unit.This message storage method is similar to the method used in it and it can greatly reduce the memory requirement. These row process results are stored in SRAM.

The memory processor unit architecture explains the row process computation part. The work it does is to compare the magnitude of the input message with the current row process intermediate result, and do the E-XOR operation to store the intermediate result and send to CWB is the general decoder architecture. The work it does is to select the proper message magnitude according to the index value, and compute the sign of the message.

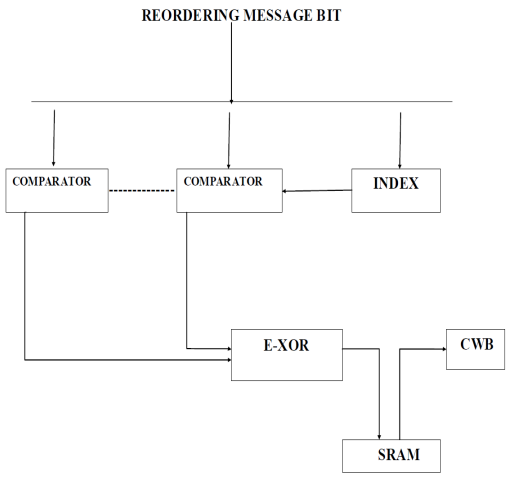

Fig.3. Message processing unit architecture

Therefore, MPU can perform the second step of th row process. At the same time, MPU is performing the second step of th row process. Such process is continued until the whole iteration is finished. For variable node processing, VPU X receives the check-toss variable message in sequential from row to, etc. The MPU communication network can also ensure that VPU X only need to receive its message from MPU .We next show the above decoding schedule more clearly with As an example, we will illustrate with the simple Universal-LDPC code matrix in Fig.3. When one iteration starts, in the first clock cycle, each MPU processes the message from a VPU according to the “1”s positions in

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the left-most sub matrix .When this one step row process is finished, the row process intermediate results are shifted.

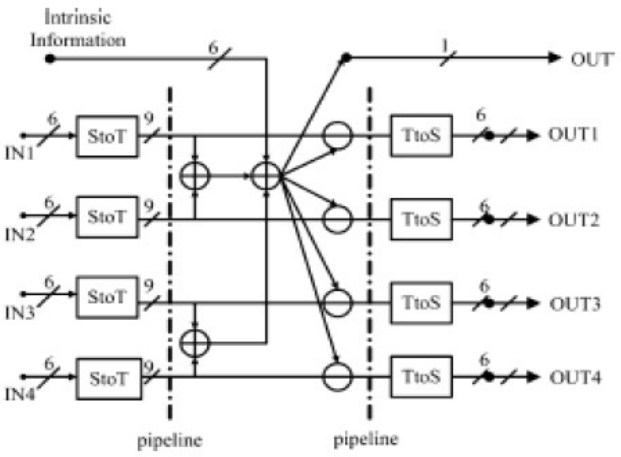


Fig.4. Virtual processing unit architecture

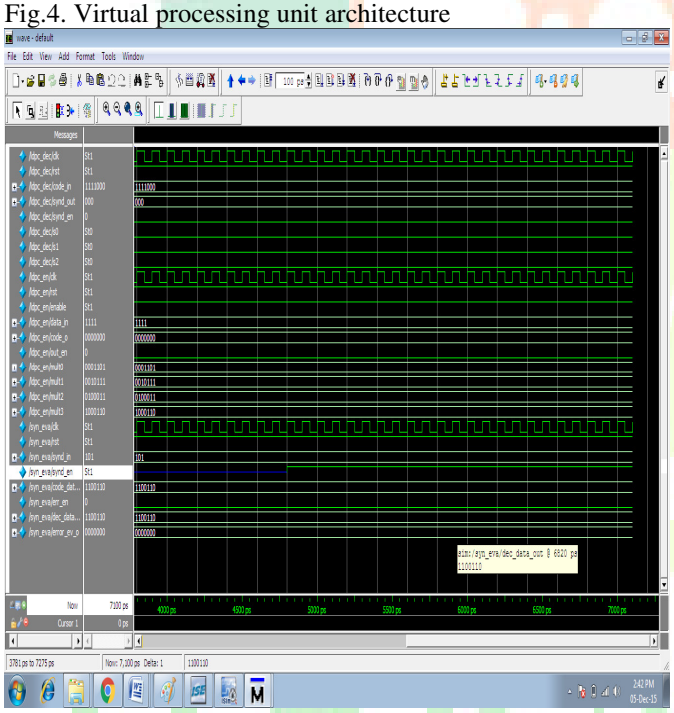
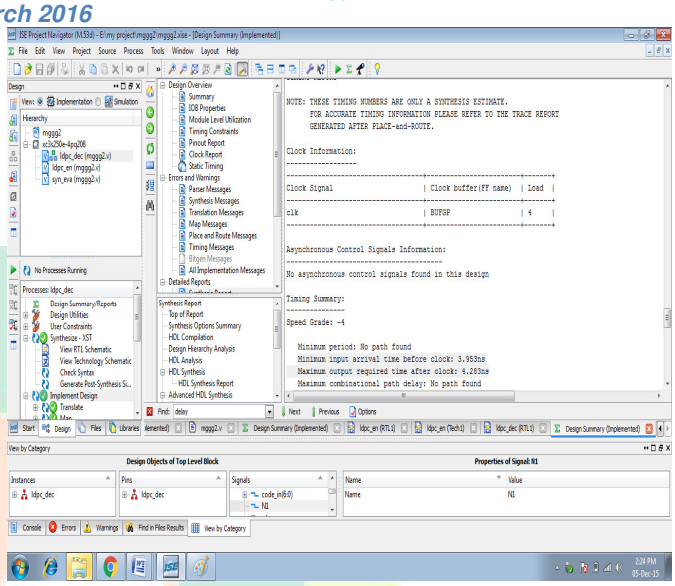


Fig.5. simulation analysis for the communication system using

VI.PERFORMANCE ANALYSIS

Compared with the existing system the throughput of the proposed system is increased up to 40% due to the introduction of low density parity check codes and fig 6 shows the delay



Delay occurred is:4.28 ns

Fig.6. performance analysis of delay for reducing error in communication system

VII.CONCLUSION AND FUTURE WORK

We have presented a general format for the implementation of Universal LDPC (Low Density Parity Check Code), and demonstrated two different bits of Universal LDPC decoders. We conclude that many of what have been considered significant disadvantages of LDPC codes (inflexibility, high encoding complexity, etc.) can be overcome by appropriate use of different algorithms and strategies that have been recently developed Loeliger et al. [2] had observed that decoders are robust to non idealities and noise in physical implementations, however they had noted that "the quantitative analysis of these effects is a challenging theoretical problem.

This work has taken steps to address this challenge by characterizing robustness to decoder noise. The extension of the density evolution method to the case of faulty decoders allows a simplified means of asymptotic performance.

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