ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com

International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2,Special Issue 6, March 2016

DESIGN AND IMPLEMENTATION OFA NEW 7&15 MULTILEVEL INVERTER TOPOLOGY

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INTRODUCTION

1.1 GENERAL

Multilevel inverters (MLIs) are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high-power applications, because improving the output waveform of the inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of Electro-Magnetic Interference generated by switching operation. Various Multi-Level Inverter structures are reported in the literature, and the Cascaded MLI appears to be superior to other inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each Full Bridge Inverter.

1.2 SCOPE OF THE PROJECT

This paper presents an overview of a new multilevel inverter topology named as reversing voltage (RV) for solar inverters. This topology requires less number of components compared to conventional topologies. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. Therefore, there is no need for all switches to work in high frequency which leads to simpler and more reliable control of the inverter.

1.3 EXISTING SYSTEM

As implementation of diodes and capacitors is there in other Multi-level Inverters (DCMLI and FCMLI). The system is operated for single DC source for obtaining high voltage levels. Symmetrical Cascaded-MLI can only be operated

for12-16 switches [S=2(m-1), where m is the number of output voltage levels, S is the number of switches].

1.4 EXISTING SYSTEMS TECHNIQUE:

A novel four-level inverter topology with even number of voltage levels is not capable of outputting a zero-voltage state. As a result, the inverter output phase voltage for zero modulation indexes is a bipolar waveform taking two distinct values and exhibits high RMS value and considerable harmonic energy concentrated at the switching frequency. This is a disadvantage of the proposed inverter, particularly when it is giving low or zero voltage to a load.

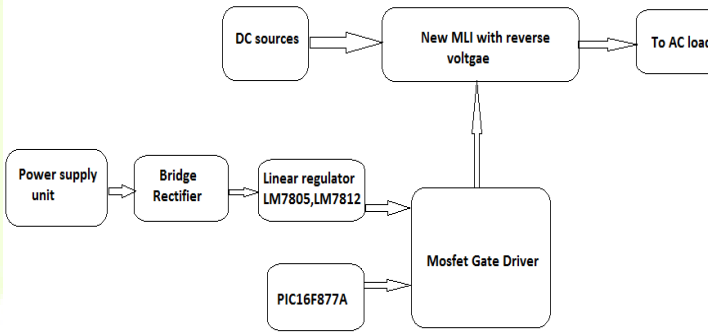
PROPOSED SYSTEM

2.1 PROPOSED SYSTEM

As implementation of diodes and capacitors is not there in Cascaded Multi-level Inverters, the voltage drops and the usage of capacitors decreases. Cascaded Multilevel inverters can only be operated only with separate DC sources. Asymmetrical MLI

can only be operated for 10-12 switches [S=(m-1)+4, where m is the number of output voltage levels, S is the number of switches.

BLOCK DIGRAM



2.1.1 PROPOSED SYSTEM TECHNIQUE

There is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is

namedlevel generation part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called polarity generation part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency. The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output.

2.1.2 ADVANTAGES OF PROPOSED TECHNIQUE

- Simple PWM Complexity

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International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2,Special Issue 6, March 2016

- Switching loss decreases.
- Usage of reactive elements is eliminated.
- Cost of the design and the installation area are reduced.

PROJECT DESCRIPTION

3.1 GENERAL

Multilevel power conversion was first introduced more than two decades ago. The general concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. There are several advantages to this approach when compared with the conventional power conversion approach. The smaller voltage steps lead to the production of higher power quality waveforms and also reduce voltage (dv/dt) stress on the load and the electromagnetic compatibility concerns. Another important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses.

3.2 MODULES NAME

- Multilevel inverter Topology
- Circuit Diagram of the project
- Operation Modes of the circuit
- Simulation Results
- Hardware Theory

3.3 MODULE DESCRIPTION

Module 1:

The power in the battery is in DC mode and the motor that drives the wheels usually uses AC power, therefore there should be a conversion from DC to AC by a power converter. Inverters can do this conversion. The simplest topology that can be used for this conversion is the two-level inverter that consists of four switches. Each switch needs an anti-parallel diode, so there should be also four anti parallel diodes. There are also other topologies for inverters.

3.3.1Cascaded Multi-level Inverter

Symmetric multilevel inverters are characterized by the fact that the voltages across the different dc link capacitors are equal. One interesting alternative is to have different capacitor voltages. This topology of inverters is known as asymmetric multilevel inverter. Although the focus for this kind of inverters has been mainly addressed in the direction of cascaded H-bridge asymmetric multilevel, asymmetric inverters can also be derived from diode-clamped and flying-capacitor inverters or a combination of them either. Asymmetric multilevel inverters have the same circuit configuration as symmetric ones. The only difference is the dc link capacitor voltages. Using different dc link voltages in different power cells and application the appropriate switching methods, the number of output voltage levels increases. Therefore, with less number of H-bridge cells, more output voltage levels can be obtained.

Circuit Diagram

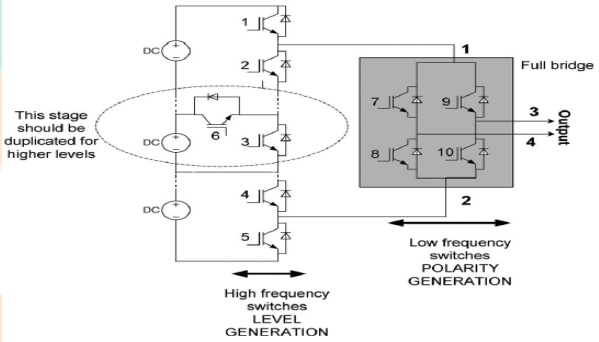

Fig.3.1. Multilevel structure of the Proposed System

3.3.2 New Multilevel Topology

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology. This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named level generationpart and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called polarity generationpart and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency.

The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities.

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Level / Mode	0	1	2	3
1	2,3,4	2,3,5	1,4	1,5
2		2,4,6	2,6,5	

Table.I. Switching Sequences for Each Level

This topology requires fewer components in comparison to conventional inverters. Another advantage of the topology is that it just requires half of the conventional carriers for SPWM controller. SPWM for seven-level conventional converters consists of six carriers, but in this topology, three carriers are sufficient. The reason is that, according to Fig.3.1, the multilevel converter works only in positive polarity and does not generate negative polarities. Therefore, it implements the multilevel inverter with a reduced number of carriers, which is a great achievement for inverter control. It is also comparable to single-carrier modulation, while this topology requires the same number of signals for PWM. However, this topology needs one modulation signal which is easier to generate as opposed to the single-carrier modulation method which needs several modulation signals.Another disadvantage of this topology is that all switches should be selected from fast switches, while the proposed topology does not need fast switches for thepolarity generation part. In the following sections, the superiority of this topology with respect to PWM switching and number of components is discussed.

3.3.3Switching Sequences

Switching sequences in this converter are easier than its counter parts. According to its inherent advantages, it does not need to generate negative pulses for negative cycle control. Thus, there is no need for extra conditions for controlling the negative voltage. Instead, the reversing full-bridge converter performs this task, and the required level is produced by the high-switching-frequency component of the inverter. Then, this level is translated to negative or positive according to output voltage requirements. This topology is redundant and flexible in the switching sequence. Different switching modes in generating the required levels for a seven-level RV inverter are shown in Table.I. The numbers show the switch according to Fig.3.1 which should be turned on to generate the required voltage level. According to the table, there are six possible switching patterns to control the inverter. It shows the great redundancy of the topology. However, as the dc sources are externally adjustable sources (dc power supplies), there is no need for voltage balancing for this work.

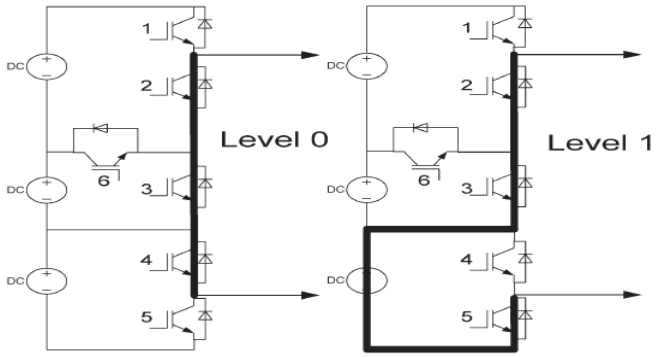

Fig.3.2 Switching Sequences For Different Level Generation

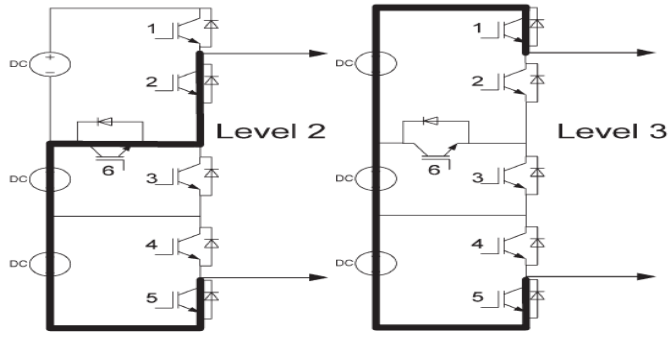

Fig.3.2 Switching Sequences For Different Level Generation

In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer. This will also help to decrease switching power dissipation. According to the aforementioned suggestions, the sequences of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) are chosen for levels 0 up to 3, respectively. These sequences are shown in Fig. 3. As can be observed from **Fig.3.2**, the output voltage levels are generated in this part by appropriate switching sequences.

The ultimate output voltage level is the sum of voltage sources, which are included in the current path that is marked in bold. In order to produce seven levels by SPWM, three saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required as shown in the next chapter. In this paper, PD SPWM is adopted for its simplicity. Carriers in this method do not have any coincidence, and they have definite offset from each other. They are also in phase with each other. The modulator and three carriers for SPWM is shown in next chapter.

States	One		two		Three	
Compare	+	-	+	-	+	-
Mode	2-3-5	2-3-4	2-5-6	2-3-5	1-5	2-5-6

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Table.I1. Switching cases in each state according to Related comparator output

The first state is when the modulator signal is within the lowest carrier. The second state is when it is within the middle carrier. Finally, the third one is when it is within the highest carrier. In each state, certain switching patterns are adopted to cover the voltage requirements. According to this definition, the switching states and switching modes are described in **Table.II**. It shows the relation between the right comparator output according to the current state and required states for switching to meet the voltage requirements. The right comparator here refers to the comparator output of the current state. As illustrated in **Table.II**, the transition between modes in each state requires minimum commutation of switches to improve the efficiency of the inverter during switching states.

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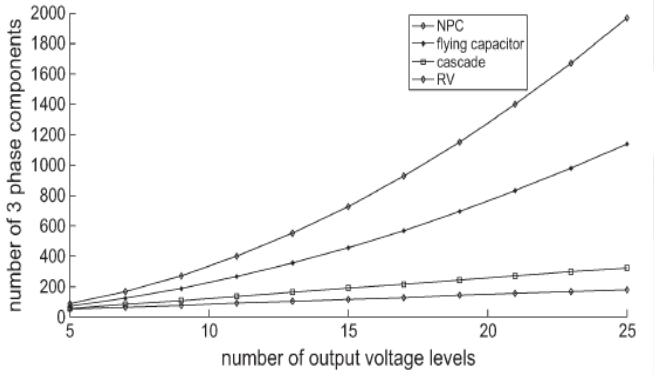

Fig.3.3. Components for multilevel inverters

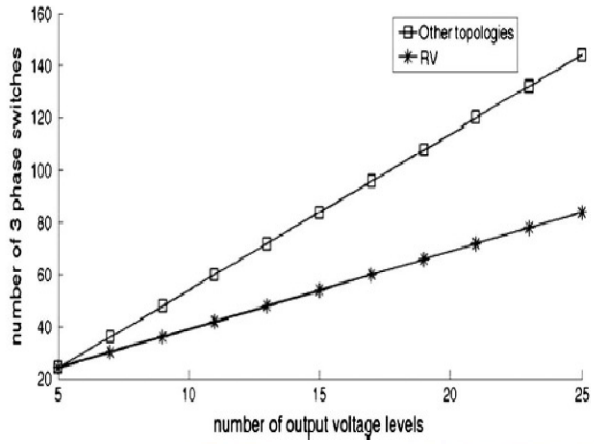

Fig.3.4. Required switches for multilevel inverter.

As the most important part in multilevel inverters is the power semiconductor switches which define the reliability and control complexity, the number of required switches against the required voltage levels is shown in **Fig.3.4** for the new topology as well as other topologies.

According to **Fig.3.3 and 3.4**, the new topology requires fewer components and also fewer switches compared to others. Therefore, it should have the potential of finding widespread applications in high-voltage power devices and apparatus that includes FACTS and HVDC. It also requires less number of components as to conventional inverters that use phase shift transformers for increasing the output voltage levels. STATCOM, which is a type of FACTS apparatus and has been widely developed in recent years, can be a good candidate for applying the topology. In order to fulfill the stringent voltage harmonic standards such as IEEE519, a STATCOM of the conventional 48-pulse inverter is normally used. The topology requires eight three-phase transformers and eight full-bridge inverters requiring 48 switches.

However, the proposed topology is superior compared to this conventional topology since it requires 84 switches for implementing similar output voltage waveform with the same quality while omitting eight bulky transformers.

Inverter type	NPC	Flying capacitor	Cascade	RV
Main switches	6(N-1)	6(N-1)	6(N-1)	3((N-1)+4)
main diodes	6(N-1)	6(N-1)	6(N-1)	3((N-1)+4)
Clamping diodes	3(N-1)(N-2)	0	0	0
DC bus capacitors/ Isolated supplies	(N-1)	(N-1)	3(N-1)/2	(N-1)/2
Flying capacitors	0	$\frac{3}{2}$(N-1)(N-2)	0	0
Total numbers	(N-1)(3N+7)	$\frac{1}{2}$(N-1)(3N+20)	$\frac{27}{2}$(N-1)	(13N+35)/2

Table III. Number Of Components For Three-Phase Inverters

SIMULATION RESULTS

4.1 TECHNIQUES USED

- Multilevel Inverter : Cascaded Asymmetrical Structure
- PDPWM

4.2 TECHNIQUES DESCRIPTION

4.2.1 Multilevel Inverter : Cascaded Asymmetrical Structure

The topology of symmetric cascaded multilevel inverter is shown in **Fig.5.1**. In this topology the output voltage of the first bridge is –Vdc, 0 or +Vdc and the output voltage of the second bridge is –Vdc, 0 or +Vdc. Therefore the output voltage of the inverter can have

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Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2,Special Issue 6, March 2016

the values 2Vdc, Vdc, 0, -Vdc, -2Vdc, which gives a five level output voltage. Asymmetric multilevel inverters as shown in **Fig.3.1** have the same topology as symmetric multilevel inverters. Thus we can change the proposed system in to asymmetrical inverter by varying the DC sources where we can analyze that the THD value increases slightly. They differ only in the rating of capacitor voltages. Each phase of a cascaded multilevel inverter requires n dc sources for 2n+1 level. For many applications it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H-bridge multilevel inverter, a scheme is proposed which uses lesser no. of bridges.

This scheme therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency.

A seven-level asymmetric cascaded H-bridge multilevel inverter has two H-bridges for each phase. Unequal dc sources are connected to the corresponding bridges. The DC source for the first H-bridge (H1) is a DC source with an output voltage of Vdc , while the DC source for the second bridge (H2) is a DC source with an output voltage of Vdc/2. The output voltage of the first H-bridge is denoted by v1 and the output voltage of the second H-bridge is denoted by v2 so that the output of this two DC source cascaded multilevel inverter V(t) = V1 (t) + V2 (t).By appropriately opening and closing the switches of H1, the output voltage of H1 can be made equal to +Vdc , 0 and –Vdc.

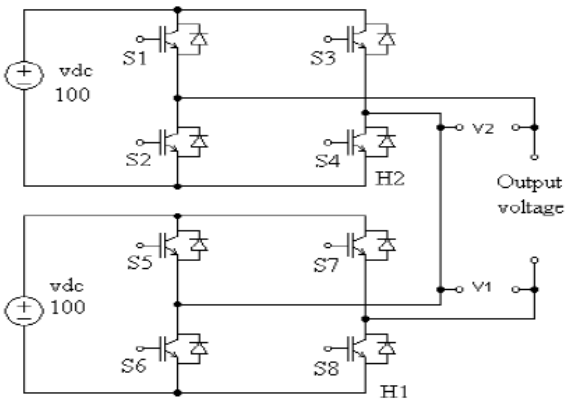

Fig.4.1. Asymmetrical Cascaded MLI

4.2.2 MODULATION STRATEGIES: PDPWM Technique

The most popular method of controlling the output voltage is by incorporating PWM control within the inverters. In this paper sixteen different modulation strategies are introduced in order to increase the output voltage and

also to reduce the THD in which the fixed DC is converted into continuous AC signal efficiently by controlling the on and off time of PWM signal. It is generally recognized that, increasing the switching frequency of the PWM pattern results in reducing lower frequency harmonics. This paper includes reference waveform as sinusoidal and (m-1)/2 triangular carriers. A popular PDPWM strategy is simulated in this work. The gate signals for chosen seven and nine level cascaded MLI are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index ma and for various PWM strategies. The simulation results presented in this work are compared and evaluated.

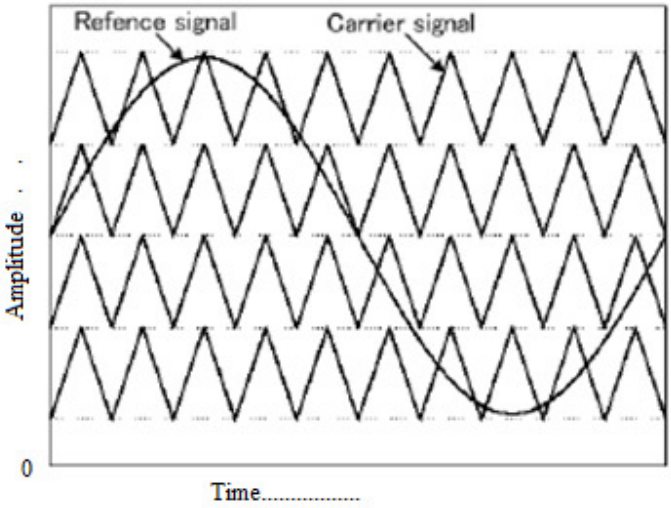

Fig.4.2. Multi-carrier based sinusoidal PWM form levels

All carrier waveforms are in phase with the identical frequency. The frequency of the modulated signal (a reference sinusoidal waveform) determines the fundamental frequency of the output current waveform,while the frequency of triangular carrier waves gives the switching frequency of the power switches. An m-level output voltage waveform using thismodulation requires (m-1)/2 triangular carriers with the same frequency.

4.3 Simulation Design without Modulation

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ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com

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A simulation designwithout modulation technique as shown in **Fig.5.3, Fig.5.6 & Fig5.9** is implemented in MATLAB SIMULINK with the help of pulse generators where the dutycycle is varied differently to obtain the 7-level (**Fig.5.4 & Fig5.7**) and 13-levels (**Fig.5.10**). A conventional 7-level system which is shown in **Fig.5.3** is also operated where the system does not operate for RV technique. A modified circuit of the system ie a 13-level inverter is also designed which is shown in **Fig.5.9**. The THD analysis is also compared for all the three simulations which isshown below in **Fig.5.5, 4.8 & 5.11.**

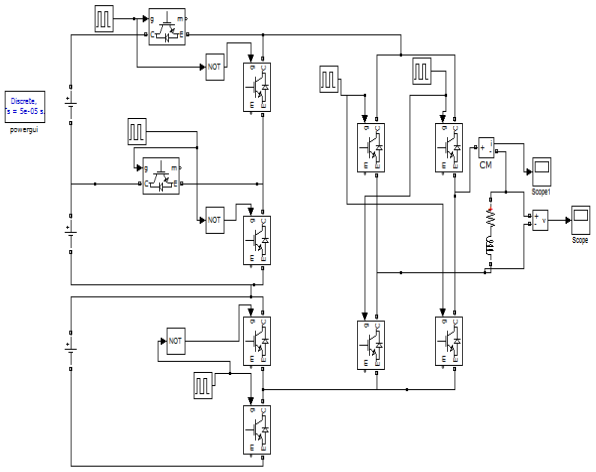

Fig.4.3. Proposed 7-level Inverter

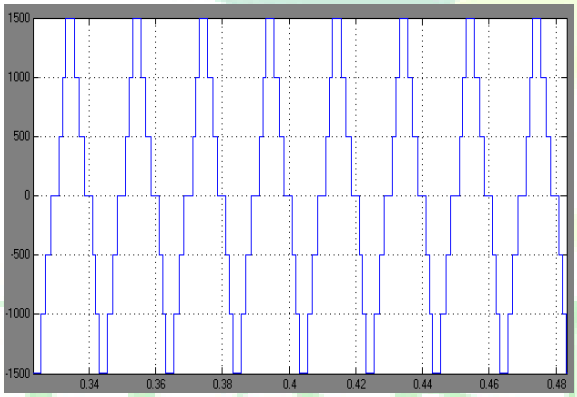

Fig.4.4. O/P 7-Level Waveform

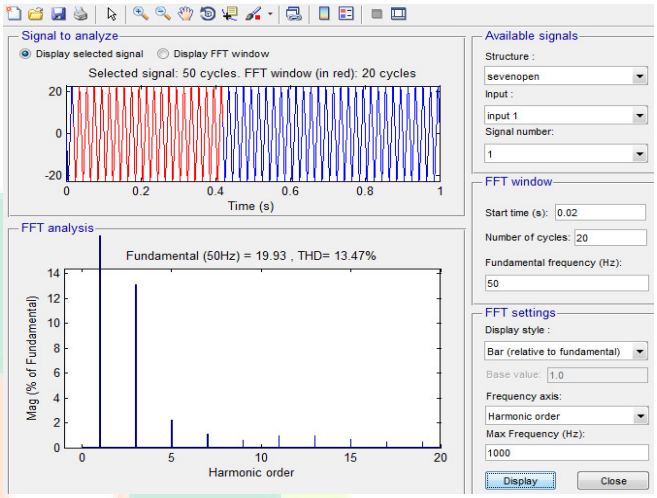

Fig.4.5. O/P Current Distortion

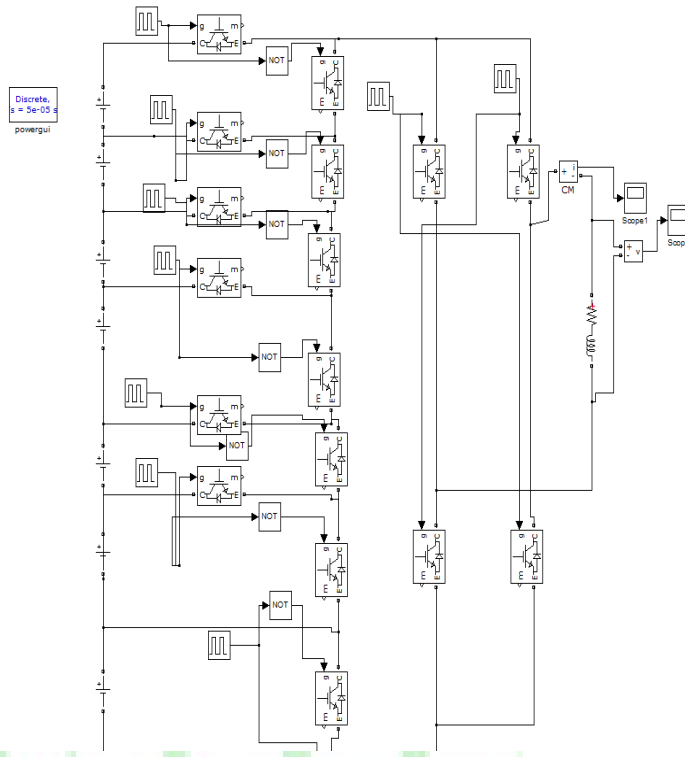

Fig.4.10 15-o/p voltage waveform

4.4 Modulation Technique

A level shifting modulation scheme PDPWM is considered. The simulation design shows three carrier waves of same frequency 2kHz compared with a reference wave (of phase shift 0º, 120º, 240º). The

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Available online at www.ijarmate.com
International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE) Vol. 2,Special Issue 6, March 2016

compared pulses is given to the IGBT switches through Goto and From signals in Matlab. The relational operator in Matlab acts as comparator. The carrier wave is generated by repeating sequence. The abs (absolute) block will omit the negative sequence of the sine wave by delivering only the positive part.

Screen shots for the simulation carried out for the proposed three phase 7 & 13 level inverter circuit under PDPWM technique.

4.5 EXPECTED INPUT AND EXPECTED OUTPUT

Here the I/P given to the circuit is 500V and the output got is 3000V for 13-level and 1500V for 7-level.

4.6 ADVANTAGES

- Simple PWM Complexity
- Switching loss decreases.
- Usage of reactive elements is eliminated.
- Cost of the design and the installation area are reduced.

5. FUTURE SCOPE

The system can be extended for more levels. Increase in more levels will sure decrease the distortions. The system has more number of DC sources that can be decreased, the modulation index can be decreased and the number of switches can be decreased.

6. CONCLUSION

In this paper, a new inverter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated DC supplies, control requirements, cost , and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV Systems, UPS, etc. The experimental results of the developed prototype for a seven-level inverter of the proposed topology are demostrated in this paper. The results clearly show that the proposed topology can effictively work as a multilevel inverter with a reduced number of carriers of PWM.