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OPTIMIZED DESIGN OF ARITHMETIC LOGIC UNIT USING MODIFIED SQUARE ROOT CARRY SELECT ADDER

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***Abstract* -- Adders in VLSI design circuits are used to design Multipliers, Arithmetic Logic Unit (ALU) and digital signal processors. Arithmetic Logic Unit (ALU) is a digital design circuit that performs arithmetic and bitwise logical operations on binary numbers. The ALU design aims to minimize time complexity for achieving high speed, as well as area complexity for cost reduction. The Square Root Carry Select Adder (SQRT CSLA) is one of the fastest adders which used as adder block in ALU. The regular carry select adder consists of ripple carry adder (RCA) with cin=0 blocks, ripple carry adder (RCA) with cin=1 blocks and multiplexer which is used to select the sum and carry obtained from RCA blocks. In order to reduce the power and area, Carry Bypass Adder (CBA) is used instead of RCA with cin=0 and series of AND gates is used instead of RCA with cin=1. The SQRT CSLA can be coded using Verilog HDL Programming Language that is simulated in XILINX ISE 14.1 simulation tool and synthesized in Cadence Encounter RTL Compiler of TMSC 0.18µm technology. The proposed SQRT CSLA is compared with regular SQRT CSLA that shows better results with a reduction in power and area. The 128-bit ALU is designed by using proposed design of SQRT CSLA.**

***Keyword*-- Arithmetic Logic Unit (ALU), RCA, Carry Bypass Adder (CBA), SQRT CSLA.**

I. INTRODUCTION

ALU is the building block element for Central Processing Unit (CPU). A number of basic arithmetic and bitwise logic operations are commonly supported by ALUs [7]. The Arithmetic operations are add such as A and B inputs are summed and the sum appears at Y output and carry-out, subtract B input is subtracted from A input (or vice-versa) and the difference appears at Y output and carry-out, multiplication and division. The Bitwise logical operations are NOT of A or B input, bitwise AND of A and B appears at Y output, bitwise OR of A and B appears at Y, bitwise XOR of A and B appears at Y. The ALU shift operations cause operand A (or B) input to shift left or right and the shifted operand appears at Y output.

Ripple carry adders (RCA) provide one of the simplest types of carry-propagate adder designs. An n-bit RCA is formed by cascading n FAs. The carry out from the kthFA is used as the carry in of the (k + 1)thFA [2]. The main advantage to this implementation is that it is efficient and easy to construct. If the implementation of circuit is simple, certain circuit may be efficiently implemented as an RCA. It increases the delay and reduces the speed of operation. The Carry Select Adder (CSLA) can be used to avoid this problem of carry propagation [4]-[5]. The regular SQRT CSLA consists of RCA with Cin=0, RCA with Cin=1and multiplexer which is used to select the sum and carry obtained from the RCA blocks [3]. The modified SQRT CSLA consists of variable sized RCA with Cin=0 blocks and Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 blocks in order to reduce the area and power [1].

The main objective of this work is to use Carry Bypass Adder (CBA) instead of RCA with Cin=0 blocks in order to reduce delay and series of AND gates is used instead Binary to Excess-1 Converter (BEC) blocks in the modified SQRT CSLA to reduce the area and power.[1]-[6]. The main advantage of the Carry Bypass Adder has reduced delay and series of AND gates have lower area and power than the regular SQRT CSLA.

This work is explained as follows. Section II presents the Binary to Excess-1 Converter (BEC) instead of using RCA with cin=1 blocks. Section III describes the detailed structural design and the function of the Carry Bypass Adder (CBA) and demonstrates the series of AND gates in place of BEC to reduce the number of logic gates. Section IV describes the structural design and operation of Arithmetic Logic Unit (ALU). Section V performs the comparison of synthesis results for different Square Root Carry Select Adder designs with regular SQRT CSLA and synthesis results of 128-bit

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ALU that used adder block as SQRT CSLA. Finally, this paper is concluded in section VI.

II.BINARY TO EXCESS-1 CONVERTER (BEC)

Binary to Excess-1 converter generates the output by incrementing one in the input that is obtained from the Carry Bypass Adder (CBA). Binary to Excess-1 Converter (BEC) is used in place of RCA with Cin=1 blocks in order to reduce the number of logic gates. (N+1)-bit BEC is used instead of using the N-bit RCA. The BEC is designed by using logic gates such as AND, NOT and XOR gates. The least significant bit of output from BEC is the NOT of input bit. The Boolean equations obtained from truth table for BEC. Similarly, find the Boolean equations of other blocks for designing the various bits of Binary to Excess-1 Converter. Fig. 1 illustrates the detailed design of 4-bit BEC which is designed from the truth table of BEC.

The Boolean Equations are

X0= ~B0
X1= B0^B1
X2= B2^ (B0&B1)
X3= B3^ (B0&B1&B0)

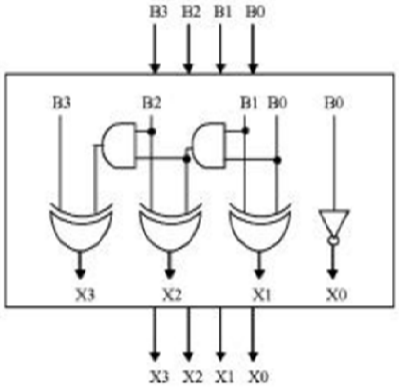

Fig.1. Binary to Excess-1 Converter (BEC)

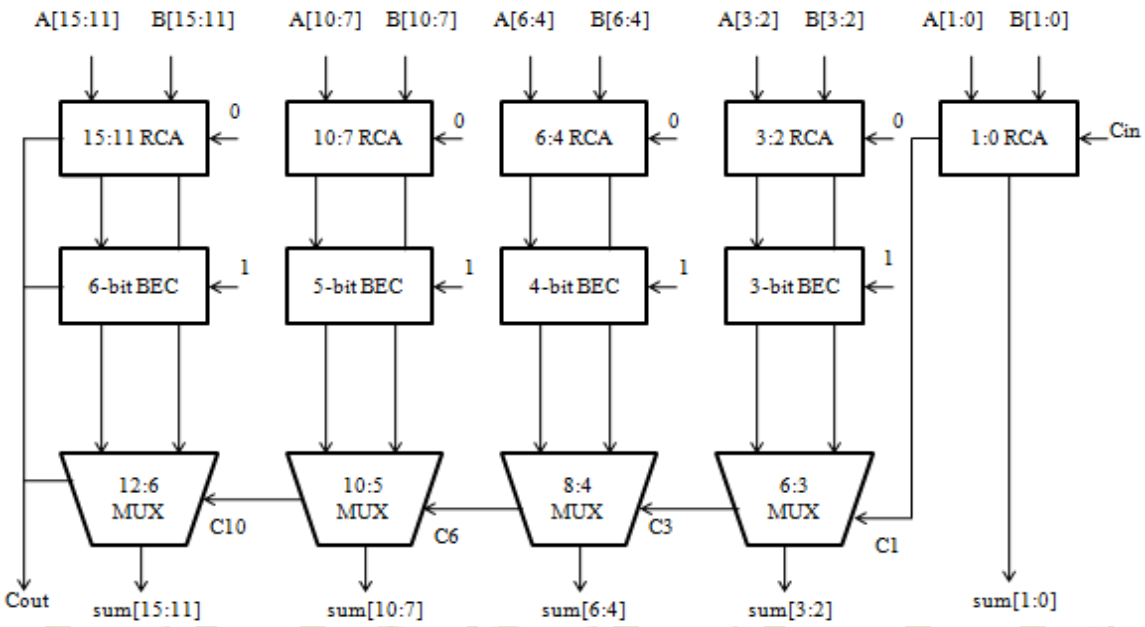

Fig. 2. 16- bit SQRT CSLA with BEC

In fig.2, it shows the block diagram of 16-bit SQRT CSLA with BEC. It describes that 4-bit BEC is used to replace the 3-bit RCA with cin=1 blocks in order to reduce the number of logic gates. It leads to reduce the power and area of SQRT CSLA.

III.CARRY BYPASS ADDER

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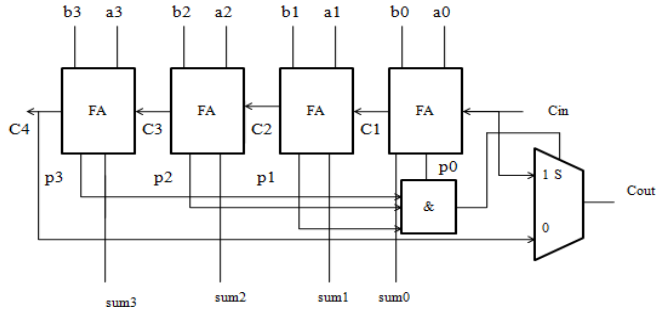

Fig. 3. Carry Bypass Adder

Carry Bypass Adder (CBA) is used for reducing the area and power compared with the regular SQRT CSLA. In fig.2, it has variable size of RCA with cin=0 blocks that is replaced by using Carry Bypass Adder (CBA). Fig.3 shows the block diagram of Carry Bypass Adder (CBA) which consists of full adders in series, one multiplexer and n-input AND-gate. Each propagate bit Pi, that is provided by the carry-ripple-chain is connected to the n-input AND-gate and resulting bit is used as the select line of a multiplexer that switches either the last carry-bit Cn or the carry-in C0 to the carry-out signal Cout. In the CBA, the operands are divided into blocks of r bit blocks. Within each block, a ripple carry adder or smaller CPA is utilized to produce the sum bits and a carry out bit for the block. It sets the carry-in signal of a block to zero causes the carry out to serve as a block generate signal. Therefore, an r bit AND gate is also used to form the block propagate signal. The block generate and block propagate signals produce the input carry to the next block. If Ai input is not equal to Bi input, carry is not generated. Hence, it is not propagated to the next block. If inputs Ai and Bi are equal to one, carry is generated which may be propagated to the output of that block. If inputs Ai and Bi are equal to zero, carry will not be propagated to the next block. This greatly reduces the delay of the adder through its critical path, since the carry bit for each block can "skip" over blocks with a group propagate signal set to logic 1. The number of inputs of the AND-gate is equal to the width of the adder.

TABLE 1

Truth Table for Carry Bypass Adder

A	B	C_i	S	C_o	*Carry status*
0	0	0	0	0	delete
0	0	1	1	0	delete
0	1	0	1	0	propagate
0	1	1	0	1	propagate
1	0	0	1	0	propagate
1	0	1	0	1	propagate
1	1	0	0	1	generate
1	1	1	1	1	generate

In table I, it illustrates the truth table for Carry Bypass Adder which gives the operation of CBA. When A and B has logic '1' input, it generates the carry which is propagated to the next full adder.

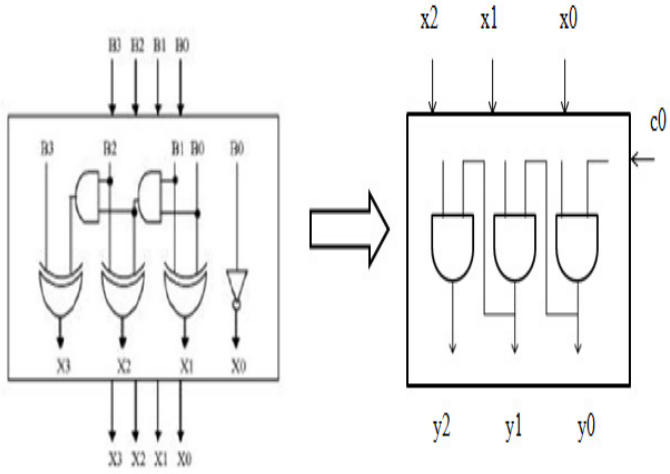

Fig. 4. Conversion of Binary to Excess Converter to series of AND gates

To replace N-bit BEC, N-1 number of AND gates are used in order to reduce the number of logic gates. In fig. 2, it explains that AND gates are connected in series instead of using Binary of Excess-1 Converter in order to reduce the power and area. As shown in fig.4, it describes the conversion of 4-bit BEC to series of 3 AND gates. In fig.5, it shows the block diagram of 16-bit SQRT CSLA with series of AND gates. The series of AND gates blocks are used instead of using BEC blocks from the block diagram of SQRT CSLA with BEC.

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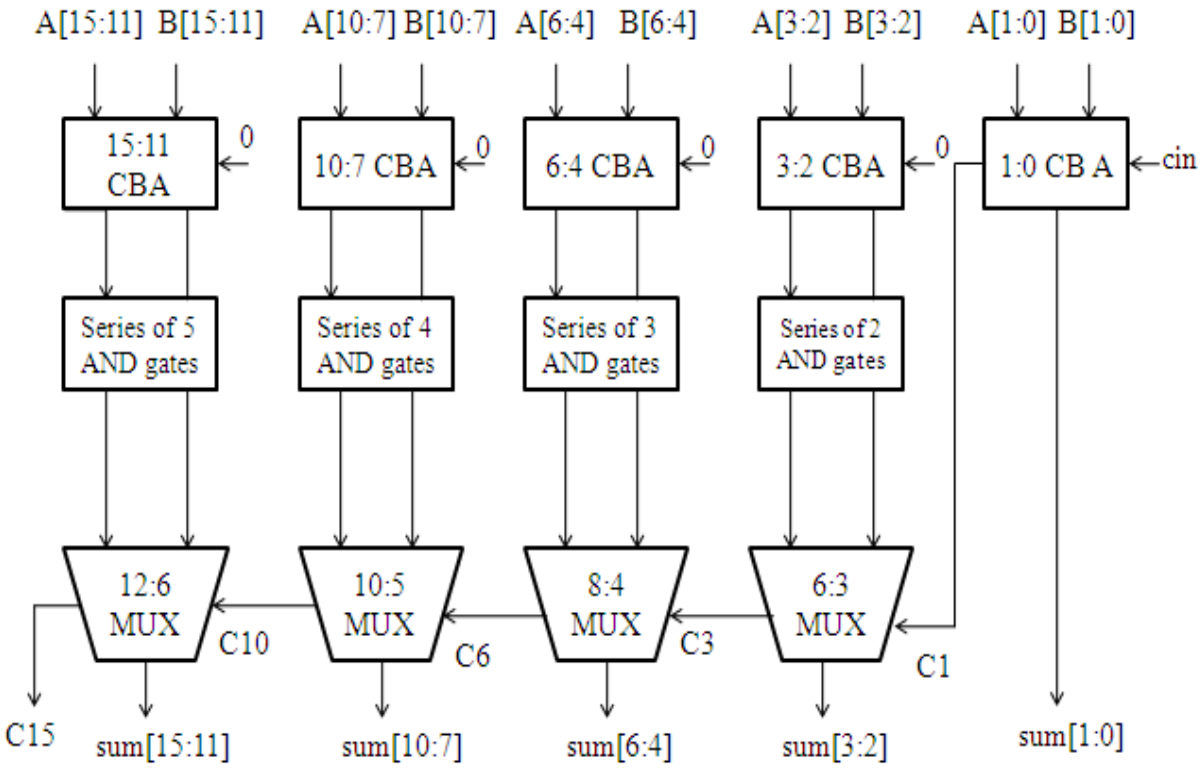

Fig.6. 16-bit SQRT CSLA with series of AND gates

IV.ARITHMETIC LOGIC UNIT (ALU)

ALU performs arithmetic operations and logical operations. A and B are input lines and S2, S1 and S0 used as a select lines which select the operations to be performed by ALU. F and Cout are outputs and carry output respectively. When 000 is used as a select line, it performs ADD operation. When 101 is used as a select line, it performs left shift operation.

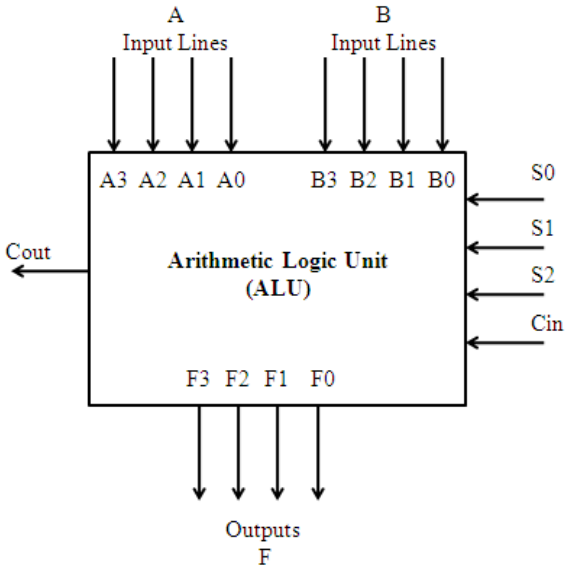

Fig.6. Block Diagram of ALU

TABLE II
Arithmetic and Logic Operations

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S2	S1	S0	Operations
0	0	0	ADD
0	0	1	SUB
0	1	0	Bitwise OR
0	1	1	Bitwise AND
1	0	0	Bitwise XOR
1	0	1	Right Shift
1	1	0	Left Shift
1	1	1	Bitwise NOT

In Fig. 7 and Table II describe the block diagram of ALU and arithmetic and logic operations respectively.

TABLE III
AREA COMPARISON

BIT	Regular SQRT CSLA	SQRT CSLA with BEC	SQRT CSLA with CBA	SQRT CSLA with series of AND gates
8-bit	1214	1007	948	835
16-bit	2704	2119	2080	1621
32-bit	5755	4327	4068	3160
64-bit	12544	9458	9033	6824
128-bit	30693	23798	23541	16712

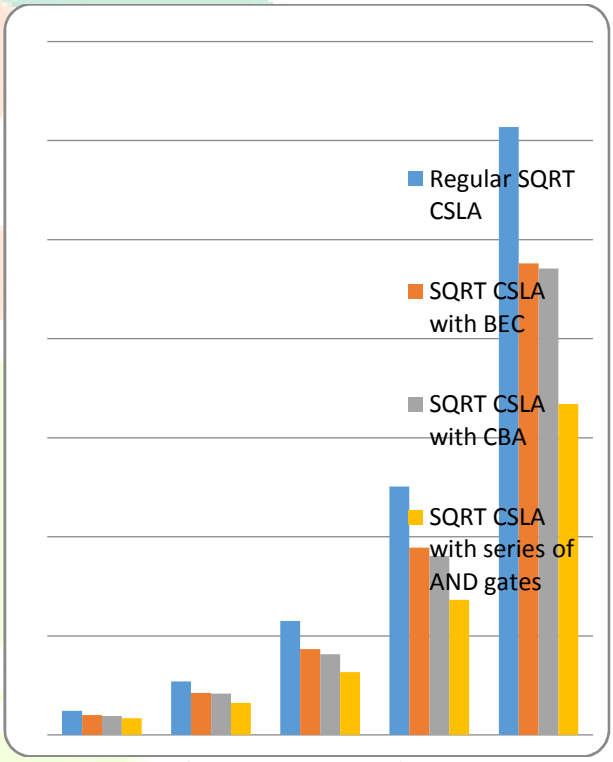

Fig. 8. Area Comparison

TABLE IV
POWER COMPARISON

BIT	Regular SQRT CSLA Power(nW)	SQRT CSLA with BEC Power(nW)	SQRT CSLA with CBA Power(nW)	SQRT CSLA with series of AND gates(nW)

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8-bit	584952.972	536290.944	514268.789	428854.393
16-bit	1369260.469	1134048.914	1024536.836	974705.972
32-bit	2940658.518	2380695.279	2270871.257	2054969.897
64-bit	6748408.758	6065880.549	5878315.085	5374810.871
128-bit	18031974.229	14330834.115	14123446.453	13089791.901

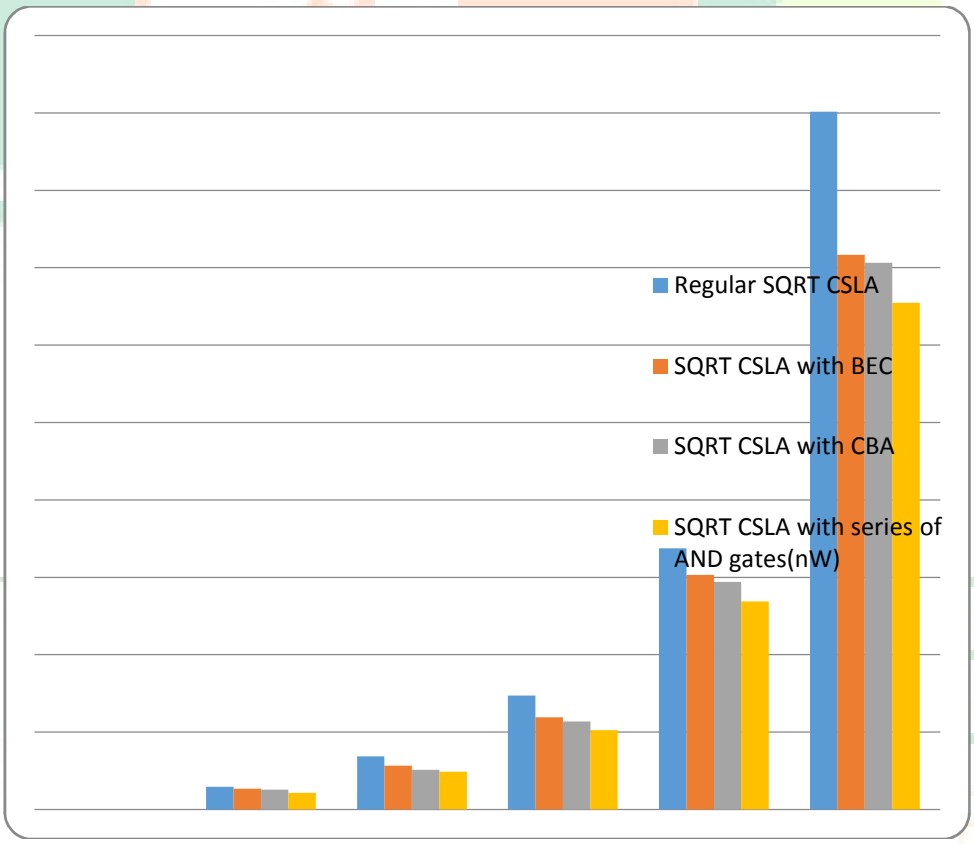

Fig. 9. Power Comparison

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TABLE V
AREA AND POWER COMPARISON FOR128-BIT ALU

Parameter	Regular SQRT CSLA	SQRT CSLA with BEC	SQRT CSLA with CBA	SQRT CSLA with series of AND gates
Area	77409	33821	33821	28734
Power	4292057 2.277	367118 5.468	367118 5.468	314238 7.669

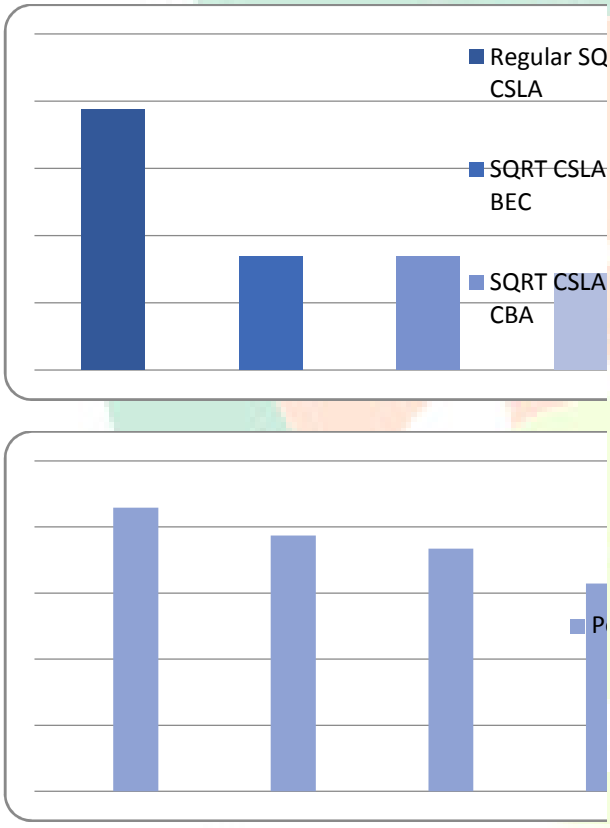

Fig. 10. ALU comparison

07%

respectively. The modified ALU architecture has low power, low area, simple and efficient for VLSI implementation. For future work, 128-bit ALU with modified SQRT CSLA will be designed by using reversible gates.

V.SYNTHESIS RESULT

The 128-bit ALU has coded using verilog Hardware Description Language (HDL) in Xilinx ISE 14.1 for regular SQRT CSLA, SQRT CSLA with BEC,SQRT CSLA with CBA and SQRT CSLA with series of AND gates. All the designs are synthesized in the Cadence Encounter RTL Compiler (RC) using the TMSC 180-nm technology. Fig. 6 illustrates the block diagram of modified 16- bit SQRT CSLA with series of AND gates. As shown in Table III and Table IV, the proposed SQRT-CSLA involves significantly consumes less power and less area than the existing designs of SQRT CSLA. Fig. 8 and fig. 9 show the graphical representation of area and power comparisons respectively. The synthesis result of Table V gives the area and power comparison of 128-bit ALU. Fig.10 shows the graphical representation of area and power comparison for different designs of SQRT CSLA present in the ALU. The area of the proposed SQRT CSLA for 8, 16, 32, 64 and 128- bit is reduced by 7.23%, 14%, 21.16%, 7.11%and 20.5% respectively. Similarly, the power of the proposed SQRT CSLA for 8, 16, 32, 64 and 128- bit is also reduced by 7%, 9%, 5%, 4.2% and 23.07% respectively. The area and power of 128-bit ALU is reduced than the existing design of ALU.

VI.CONCLUSION

In VLSI design process, area, power and delay are the important factors that determine the performance of any circuit. This paper designed the 128-bit ALU which has different designs of SQRT CSLA with reduction in area and power that can be compared with the regular ALU design. The SQRT CSLA using Carry Bypass Adder and series of AND gates shows better performance in terms of area, power and delay than the ripple carry adder. The area and power of the modified design for 128-bit ALU is reduced by 20.5% and 23.

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