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AN EFFICIENT POWER BARREL LEVEL SHIFTER FOR NEAR THRESHOLD CIRCUITS EXHIBITS SHORTER DELAY

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Abstract—Energy efficiency is a primary concern in modern sub-30-nm CMOS microprocessors. A standard method to reduce dynamic power consumption is to lower the supply voltage due to the quadratic dependence of dynamic power on voltage. A negative temperature coefficient has, therefore, become an attractive methodology for sub-30-nm CMOS circuits. This mode of operation is characterized by a balance between speed and power. By operating a circuit near the threshold voltage as compared with a much lower voltage deep within the sub threshold region, a balanced approach to managing power is achieved while maintaining a reasonable circuit delay.

I. INTRODUCTION

1.1 A Wide-Range Level Shifter Using a Modified Wilson Current Mirror Hybrid Buffer

Wide-range level shifters play critical roles in ultralow-voltage circuits and systems. Although state-of-the-art level shifters can convert a sub threshold voltage to the standard supply voltage, they may have limited operating ranges, which restrict the flexibility of dynamic voltage scaling. Therefore, this paper presents a novel level shifter, of which the operating range is from a deep sub threshold voltage to the standard supply voltage and includes upward and downward level conversion.The proposed level shifter is a hybrid structure comprising a modified Wilson current mirror and generic CMOS logic gates. The simulation and measurement results were verified using a 65-nm technology. The minimal operating voltage of the proposed level shifter was less than 200 mV based on the measurement results. In addition to the operating range, the delay, power consumption, and duty cycle of the proposed level shifter were designed for practical applications.

1.2 A Sub threshold to Above-Threshold Level Shifter Comprising a Wilson Current Mirror

A novel level shifter circuit that is capable of converting sub threshold to above-threshold signal levels. In contrast to other existing implementations, it does not require a static current flow and can therefore offer considerable static power savings. The circuit has been optimized and simulated in a 90-nm process technology. It operates correctly across process corners for supply voltages from 100 mV to 1 V on the low-voltage side. At the target design voltage of 200 mV, the level shifter has a propagation delay of 18.4 ns and a static power dissipation of6.6 nW. For a 1-MHz input signal, the total energy per transition is93.9 fJ. Simulation results are compared to an existing sub threshold to above-threshold level shifter implementation from the paper of Chen *et al.*We have presented a new sub threshold to above-threshold level shifter circuit based on a Wilson current mirror. The circuit does not have a static current path between the supply rails and therefore offers reduced static power dissipation. The simulation results of the level shifter in a 90-nm process technology.

1.3 Low-Power Level Shifter for Multi-Supply Voltage Designs

A new low-power level shifter (LS) is presented for robust logic voltage shifting from near/sub-threshold to above-threshold domain. The new circuit combines the multi threshold CMOS technique along with novel topological modifications to guarantee a wide voltage conversion range with limited static power and total energy consumption. When implemented in a 90-nm technology process, the proposed design reliably converts 180-mV input signals into 1-V output signals, while maintaining operational frequencies above 1-MHz, also taking into account process-voltage-temperature variations. Post-layout simulation results demonstrate that the new LS reaches a propagation delay less than 22 ns, a static power dissipation of only 6.4 nW, and a total energy per transition of only 74 fJ for a 0.2-V 1-MHz input pulse.

1.4 An Energy-Efficient Sub threshold Level Converter in 130-nm CMOS

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A fast energy-efficient level converter capable of converting an input signal from sub threshold voltages up to the nominal supply voltage. Measured results from a 130-nm test chip show robust conversion from 188 mV to 1.2 V with no intermediate supplies required. A combination of circuit methods makes the converter robust to the large variations in the current characteristics of sub threshold circuits. To support dynamic voltage scaling, the level converter can up convert an input at any voltage within this range to 1.2 V.Typical and slow are simulated from the two process corners TT and SS. The experimental delay is within the range of both the typical and slow simulations.To verify its effectiveness and capabilities, we implemented the level converter in a bulk CMOS 130-nm test chip.

1.5 Fast and Wide Range Voltage Conversion in Multi supply Voltage Designs

Multi supply voltage design technique is widely used in modern system-on-chips to trade off energy and speed. Level shifters (LSs) allow different voltage domains to be interfaced. In this brief, new LS is presented for fast and wide range voltage conversion. Because of a novel architecture combined with the use of multi threshold CMOS technique, the proposed circuit guarantees robust voltage shifting from the deep sub threshold to the above-threshold domain while exhibiting fast response and low energy consumption. When implemented in a 90-nm technology node, considering process-voltage-temperature variations, the proposed design reliably converts 100-mV input signals into 1 V output signals. Post-layout simulation results demonstrate that the new LS shows a propagation delay of 16.6 ns, a static power dissipation of 8.7 nW and a total energy per transition of only 77 fJ for a 0.2 V 1-MHz input pulse.New LS suitable for robust logic voltage shifting from near/sub threshold to above-threshold domain has been presented. The proposed circuit exploits proper design strategies to increase the operating speed while maintaining very low energy consumption and large voltage conversion range. When used to up-convert voltage signals from the deep sub threshold regime, the novel design outperforms all the previously proposed LSs.

1.6 Near-Threshold-Voltage Circuit Design: The Design Challenges and Chances

NTV is a new low power design concept for the pursuit of the highest power usage efficiency. The characteristics for each logic family are quite different under NTV while comparing to its operation under normal supply voltage. The circuit/architecture design policy under NTV is also different from its normal supply voltage operation. Process variation, performance degradation, and noise-interference are the three major design challenges in NTV design. In this paper, some effective candidate design solutions are presented to overcome these crucial NTV issues. In the NTV circuit design, how to lower its process variation is the most important issue. Dynamic logic family circuits may still have good chance because of high speed and delay variation insensitive superiority; however, its signal contention and leakage problems should be solved in advance.

1.7 Novel Wide Voltage Range Level Shifter For Near-threshold Designs

A novel low-to-high level shifter that enables having voltage domains with substantially different supply voltages from near-threshold to full supply voltage. The level shifter was designed in a 90nm CMOS technology and uses thick oxide transistors, non-minimum channel length transistors, along with novel circuit structures to up convert from 0.36V to 1.32V and all the voltage levels in between for all process corners and the temperature range of [O°C -125°C]. Relaxing the temperature operating range to [25°C -125°C], the level shifter works deep into the sub threshold region capable of up converting from 0.31 V to 1.32 V. For the typical case operating condition, the proposed level shifter has an unprecedented performance of 1.5 ns while up converting 0.36V to 1.32V...

1.8 Near-Threshold Computing: Reclaiming Moore's Law through Energy Efficient Integrated

Power has become the primary design constraint for chip designers today. While Moore's law continues to provide additional transistors, power budgets have begun to prohibit those devices from actually being used. To reduce energy consumption, voltage scaling techniques have proved a popular technique with sub threshold design representing the endpoint of voltage scaling. Although it is extremely energy efficient, sub threshold design has been relegated to niche markets due to its major performance penalties. It defines and explores near-threshold computing (NTC), a design space where the supply voltage is approximately equal to the threshold voltage of the transistors. This region retains much of the energy savings of sub threshold operation with more favourable performance and variability characteristics.This makes it applicable to a broad range of power-constrained computing segments from sensors to high performance servers. This paper explores the barriers to the widespread adoption of NTC and describes current work aimed at overcoming these obstacles. As Moore's law continues to provide designers with more transistors on a chip, power budgets are beginning to limit the applicability of these additional transistors in conventional CMOS design.

II. PROPOSED SYSTEM

This system explains techniques such as dynamic voltage scaling operating down to near threshold voltage levels and supporting multiple voltage domains have become necessary to reduce dynamic as well as static power. A key component of these techniques is a level

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shifter that serves different voltage domains. This level shifter must be high speed and power efficient. The proposed level shifter translates voltages ranging from 250 to 790 mV, and exhibits 42% shorter delay, 45% lower energy consumption, and 48% lower static power dissipation. In addition, the proposed level shifter exhibits symmetric rise and fall transition times with up to 12% skew at the extreme conditions over the maximum range of voltages.

For all the above work describes threshold voltage levels in FET and improve efficient of the digital circuit by using Barrel Level Shifter. 8:1 multiplexer is used to achieve level shifter in FET. Additionally we implement the Barrel Level shifter which performs left shift, right shift and rotational shift. Shift operation is done by Select lines from MUX. Power efficiency of FET is reduced by switch OFF unused FET in the digital circuit. This is done by level shifting to OFF state by using select lines. Thus it reduces the energy consumption up to particular percentage.The speed and tolerance to variations at low voltage levels are arguably the most important issues in near threshold circuits. To demonstrate the feasibility of this level shifter for low voltage operation, the proposed circuit is validated against statistical Monte Carlo analysis with 1,000 iterations. The Monte Carlo analysis is applied for a range of standard corners, typical–typical (TT), slow–fast (SF), and fast–slow (FS), at 125 °C and −30 °C. The low voltage input of the level shifter is buffered with a pair of low voltage inverters to isolate the ideal voltage source and to introduce variations. These input buffers also contribute a non ideal input slew equal to 60 ps, on average, for the maximum conversion range. The output of the level shifter is connected to a fan-out load of four, which consists of four identical inverters supplied with a nominal voltage of 0.79 V. The Monte Carlo analysis at different process corners, as reported in Table I, is performed on a pre layout circuit; the simulation is, therefore, supplied with a pre extraction net list. The simulation at nominal operating conditions is performed on a post layout circuit and includes extracted parasitic impedances.

Extensive Monte Carlo analysis is carried out on the level shifter and includes the intermediate voltage generator as an internal block. The delay and energy are described separately for both rise and fall transitions. The delay is the time from the50% input transition to the 50% output transition. The energy per transition is measured from the 10% input transition to the 90% output transition. For the rising transition, the input of the level shifter changes from 0 to 250, 350, and 500 m Vlow voltage domain, whiles the output, correspondingly, changes from 0 to 790 mV. Similarly, during the falling transition, the input of the level shifter changes from 250, 350, and 500 mV to 0, while the output changes from 790 to 0 mV. Three voltage conversions are 250 to 790, 350 to 790, and 500 to 790 mV, respectively. In addition, the proposed level shifter can translate input voltages <200 mV. For these low voltages, however, part of the 1,000 Monte Carlo simulations fails to demonstrate the correct output voltage at the end of the 1-ns period. The static power dissipation is also not listed, since the proposed level shifter does not dissipate significant short-circuit power, and the intermediate voltage generator leaks an insignificant amount of current due to the large number of serially connected transistors. As an example, two Monte Carlo simulations at a maximum operating temperature of 125 °C for the nominal TT corner. The proposed level shifter exhibits good symmetry between the rise and fall transition times over all corner cases for the maximum voltage conversion range with an average difference of 4% and a worst case difference of 7%. This symmetry degrades for shorter conversion ranges. For the 500 to 790 mV conversion range, the fall time is up to twice longer than the rise time. With respect to the maximum voltage conversion range, the standard deviation is within 12% for the best case corners and within 23% for the worst case corners.

2.1 BLOCK DIAGRAM

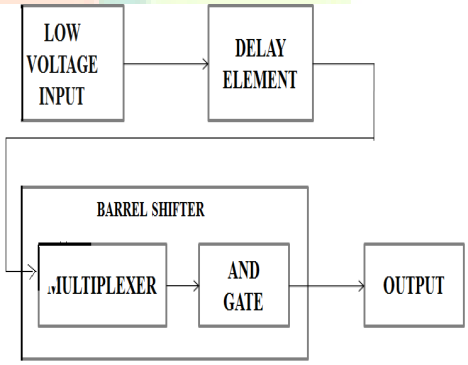

Fig: 2:1 proposed barrel level shifter

2.2 DESCRIPTION

2.2.1 DELAY ELEMENT

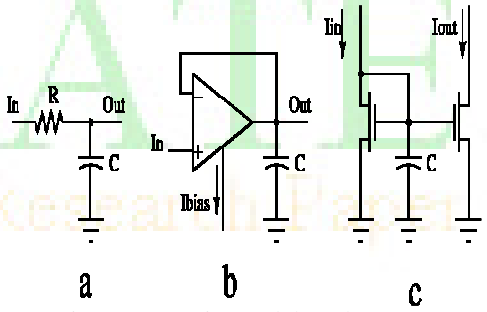

Fig: 2.2: Continues delay elements

A component which provides a specified delay bet

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ween actuation of the propellanactuated devices and ignitio n of the propellant. An explosive train component consisting of a primer, a delay column, and a relay transfer charge assembled in a single housing to provide a controlled time delay.

2.2.2 MULTIPLEXER

In electronics, a multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output.Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. An electronic multiplexer makes it possible for several signals to share one device or resource, for example one A/D converter or one communication line, instead of having one device per input signal.

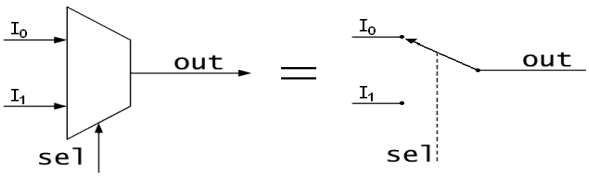
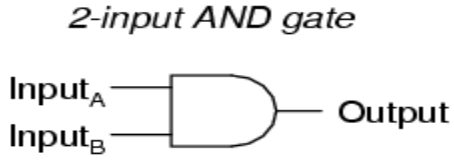


Fig: 2.2: Multiplexer

2.2.3 AND GATE

AND gate is a basic digital logic gate that implements logical conjunction - it behaves according to the truth table to the right.



A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Fig: 2:3 2-Input AND Gate

2.2.4 LEVEL SHIFTER

A level shifter is usually a part that converts digital signals from one logic standard to another. It might also be called a *translator*. For example, the MC14504B converts TTL logic signals to CMOS levels, and a MC10H607 converts PECL signals to TTL. A level shifter isn't meant to provide power, it can only source as much current as its target logic levels require.The terms *voltage regulator* and *dc-dc converter* are somewhat overlapping. Classic linear regulators are almost always called *regulators*. Linear regulators can only be used to produce a lower voltage from a higher one. Switching supply circuits might be called *regulators* or *dc-dc converters*.

2.2.5 BARREL LEVEL SHIFTER

Barrel Shifter plays an important role in the data shifting and data rotation. It is having application in many areas. The Barrel Shifter is mainly use for the simplification of the data shifting.The Arithmetic and the Logical Shifters can also be replaced by the Barrel Shifter Because with the rotation of the data it also provide the application the data right, left shifting either arithmetically or logically. The purpose of this is to design the two bit barrel shifter using universal gates with the help of CMOS logic and the most important two 2:1 multiplexers (mux). The further advanced version of the barrel Shifter is 4 bit data shifting, which is also proposed here. In this different design methodologies are used such as standard cell based design, semicustom design and full custom design of the Barrel Shifter to reduce area, power and size of the circuit. The paper analyzes and optimizes area and power of the Barrel Shifter using 45 nm technologies.

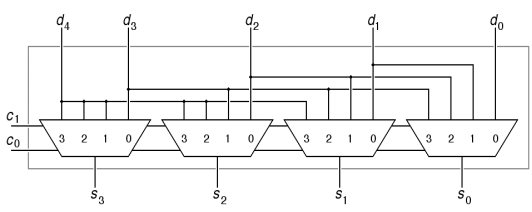


Fig 2.4: Barrel Level Shifter

A barrel shifter is a digital circuit that can shift a data word by a specified number of bits in one clock cycle. It can be implemented as a sequence of multiplexers , and in such an implementation the output of one mux is connected to the input of the next mux in a way that depends on the shift distance.

III. CONCLUSION

The proposed level shifter is shown to be suitable for integration in sub-30-nm multi voltage domain microprocessors. Extensive Monte Carlo analysis demonstrates that the proposed circuit reliably level shifts voltages between 250 and 790 mV. The proposed converter,

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therefore, supports near threshold circuits despite the increased sensitivity to process variations. The converter maintains symmetric rise and fall transition times over the maximum voltage conversion range across different statistical corners. In addition, the proposed converter is compared with recently published level shifters and exhibits significant improvements in speed, energy, and power efficiency.

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