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LEVEL-CONVERTING RETENTION FLIP-FLOP FOR REDUCING STANDBY POWER IN ZIGBEE SOCS

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Abstract—This paper proposes a simple and efficient Montgomery multiplication algorithm such that the low-cost and high-performance Montgomery modular multiplier can be implemented accordingly. The proposed multiplier receives and outputs the data with binary representation and uses only one-level carry-save adder (CSA) to avoid the carry propagation at each addition operation. This CSA is also used to perform operand pre computation and format conversion from the carry save format to the binary representation, leading to a low hardware cost and short critical path delay at the expense of extra clock cycles for completing one modular multiplication To overcome the weakness, a configurable CSA (CCSA), which could be one full adder or two serial half-adders, is proposed to reduce the extra clock cycles for operand pre computation and format conversion by half. In addition, a mechanism that can detect and skip the unnecessary carry-save addition operations in the one level CCSA architecture while maintaining the short critical path delay is developed. As a result, the extra clock cycles for operand pre computation and format conversion can be hidden and high throughput can be obtained. Experimental results show that the proposed Montgomery modular multiplier can achieve higher performance and significant area–time product improvement when compared with previous designs. In addition, a mechanism that can detect and skip the unnecessary carry-save addition operations in the one-level CCSA architecture while maintaining the short critical path delay is developed. In addition, a mechanism that can detect and skip the unnecessary carry-save addition operations.

I. INTRODUCTION

1.1 A Fully Integrated 2.4-Ghz IEEE 802.15.4 Compliant Transceiver for Zigbee Applications

A single-chip 2.4-GHz CMOS radio transceiver with integrated baseband processing according to the IEEE 802.15.4 standard is presented. The transceiver consumes 14.7 mA in receive mode and 15.7 mA in transmit mode. The receiver uses a low-IF topology for high sensitivity and low power consumption, and achieves 101 dBm sensitivity for 1% packet error rate. The transmitter topology is based on a PLL direct-modulation scheme. Optimizations of architecture and circuit design level in order to reduce the transceiver power consumption are described. Special attention is paid to the RF front-end design which consumes 2.4Ma in receive mode and features bidirectional RF pins. The 5.77 mm2 chip is implemented in a standard 0.18mCMOStechnology. The transmitter delivers +3 dBm into the 100- differential antenna port. A single-chip 2.4-GHz CMOS radio transceiver with integrated baseband processing according to the IEEE 802.15.4 standard is presented. The transceiver consumes 14.7 mA in receive mode and 15.7 mA in transmit mode. The receiver uses a low-IF topology for high sensitivity and low power consumption, achieves -101 dBm sensitivity for 1% packet error rate. The transmitter topology is based on a PLL direct-modulation scheme. Optimizations of architecture and circuit design level in order to reduce the transceiver power consumption are described. Special attention is paid to the RF front-end design which consumes 2.4mA in receive mode. The transceiver consumes 14.7 mA in receive mode and 15.7 mA in transmit mode.

1.2 A Comparative Study Of Wireless Protocols: Bluetooth, UWB, Zigbee, And Wi-Fi

Bluetooth (over IEEE 802.15.1), ultra-wideband (UWB, over IEEE 802.15.3), ZigBee (over IEEE 802.15.4), and Wi-Fi (over IEEE 802.11) are four protocol standards for short-range wireless communications with low power consumption. From an application point of view, bluetooth is intended for a cordless mouse, keyboard, and hands-free headset, UWB is oriented to high-bandwidth multimedia links, ZigBee is designed for reliable wirelessly networked monitoring and

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control networks, while Wi-Fi is directed at computer-to-computer connections as an extension or substitution of cabled networks. In this paper, we provide a study of these popular wireless communication standards, evaluating their main features and behaviours in terms of various metrics, including the transmission time, data coding efficiency, complexity, and power consumption. It is believed that the comparison presented in this paper would benefit application engineers in selecting an appropriate protocol. (UWB, over IEEE 802.15.3), ZigBee (over IEEE 802.15.4), and Wi-Fi (over IEEE 802.11) are four protocol standards for short-range wireless communications with low power consumption. From an application point of view, Bluetooth is intended for a cordless mouse, keyboard, and hands-free headset, UWB is oriented to high-bandwidth multimedia links, ZigBee is designed for reliable wirelessly networked monitoring and control networks, while Wi-Fi is directed at computer-to-computer connections as an extension or substitution of cabled networks. In this paper, we provide a study of these popular wireless communication standards, evaluating their main features and behaviors in terms of various metrics, including the transmission time, data coding efficiency, complexity, and power consumption. It is believed that the comparison presented in this paper would benefit application engineers in selecting an appropriate protocol. One of theincreasingly important components in factory automation is the industrial communication . For interconnection purposes, a factory automation system can be combined with various sensors, controllers, and heterogeneous machines.

1.3 Increasing Sleep-Mode Efficiency By Reducing Battery Current Using A DC-Converter

Battery current is a key parameter that decides the runtime of a portable electronic system. For low power applications like IEEE 802.15.4 and Zigbee wireless network, the average battery current drain approximates the sleep mode current drain, since significantly more time is spent in sleep than in active usage. This paper proposes substituting a DC-DC converter for a low drop-out (LDO) regulator in thesleep mode power chain, such that the current drawn from the battery would be less than the actualcurrent drained by the load. The battery current saving, be around 35% based on the analysis of a 65 nm CMOS IEEE 802.15.4/Zigbee low power wireless system-on-chip model, whose parameters are extracted from state-of-the-art industrial products and experimental data from advanced nanometer processes.This paper proposes substituting a DC-DC converter for a low drop-out (LDO) regulator in thesleep mode power chain, such that the current drawn from the battery would be less than the actualcurrent drained by the load. It is believed that the comparison presented in this paper would benefit application engineers in selecting an appropriate protocol. Battery current is a key parameter that decides the runtime of a portable electronic system. For low power applications like IEEE 802.15.4 and Zigbee wireless network, the average battery current drain approximates the sleep mode current drain, since significantly more time is spent in sleep than in active usage. This paper proposes substituting a DC-DC converter for a low drop-out (LDO) regulator in the sleep mode power chain, such that the current drawn from the battery would be less than the actual current drained by the load. The battery current saving, and hence battery runtime extension, is estimated to be around 35% based on the analysis of a 65 nm CMOS IEEE 802.15.4/Zigbee low power wireless system-on-chip (SoC) model, whose parameters are extracted from state-of-the-art industrial products and experimental data from advanced.

1.4 Passive Wake-Up Scheme for Wireless Sensor Networks

In resource limited mobile computing devices (wireless sensor networks), energy saving is a critical design task. However, existing wake-up mechanisms encounter a critical trade-off between energy consumption and response time. In this paper, we propose a passive RF wake up (PRFW) scheme instead of time-based scheme to wake up node that indeed needs to wake up. The PRFW scheme is enabled by a PRFW hardware module sensing radio signal from other nodes. Analysis of energy consumption and delay shows that the power saving capability and wake-up delay can be improved by using the PRFW scheme. In this paper, existing wake-up mechanisms encounter a critical trade-off between energy consumption and response time.

1.5 In Ultra Low-Power CMOS Transceiver Using Various Low-Power Techniques For LR-WPAN Applications

An implemented and evaluated a fully integrated2.4GHz CMOS RF transceiver usingvarious low-power techniques for low-rate wireless personal area network (IEEE 802.15.4 LR_WPAN) applications in 0.18-μm CMOS technology. In order to achieve an ultra low power consumption, a RC oscillator (OSC) operating below 200 nA, a regulator operating below 200 nA for sleep mode, a quick start block for the crystal oscillator, a passive wake-up circuit, a LNA with negative gm, a current bleeding mixer, and a stacked VCO are all implemented in this transceiver. The transmitter achieves less than 5.0% error vector magnitude (EVM) at 5 dBm output, and the receiver sensitivity is -101 dBm. The sensitivity of the wake-up block is -29.8 dBm. The current consumption is below 14.3 mA for the data receiving mode, 16.7 mA for the transmitter, and less than 600 nA for the sleep mode from a 1.8 V power supply. It describes the research motivating the creation of the WISP, its development process, the decision to open source its design, and the creation of the WISP Challenge, a program to make WISPs available to univer-sity researchers. The article then surveys WISP-related research performed by the author's

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group, by collaborators, and by others who received WISPs through the WISP Challenge or via other channels.

1.6 Data Centric Storage In Zigbee Wireless Sensor Networks

Data Centric Storage is a recent paradigm that results more efficient than other storage techniques. In this work we consider the use of this storage paradigm in WSN based on the ZigBee standard. In particular we propose a novel protocol (Z-DaSt) that exploits the routing and addressing features of ZigBee (that are based on routing trees) to distribute data to the sensors. The protocol also features Quality of Service in the storage of data by enabling the user to specify the amount of redundancy to be used in the storage of each datum. Analysis of energy consumption and delay shows that the power saving capability and wake-up delay can be improved by using the PRFW scheme. The PWUC consists of a receiving antenna, RF rectifier and impedance matching circuitry. This work evaluates Z-DaSt by analysis and simulation, and compares its performance to DCS-GHT. The simulation results show that Z-DaSt is a viable alternative to DCS-GHT for practical cases, in particular for low to moderate network densities.

1.7 A 1-V High-Speed MTCMOS Circuit Scheme for Power-Down Application Circuits

This paper proposes a new multi threshold-voltage CMOS circuit (MTCMOS) concept aimed at achieving high-speed, ultralow-power large-scale integrators (LSI's) for battery-driven portable equipment. The “balloon & rdquo; circuit scheme based on this concept preserves data during the power-down period in which the power supply to the circuit is cut off in order to reduce the standby power. Low-power, high-speed performance is achieved by the small preserving circuit which can be separated from the critical path of the logic circuit. This preserving circuit is not only three times faster than a conventional MTCMOS one, but it consumes half the power and takes up half the area. Using this scheme for an LSI chip, 20-MHz operation at 1.0 V and only a few nA standby current was achieved with 0.5-μm CMOS technology. Moreover, this scheme is effective for high speed and low-power operation in quarter-micrometer and finer devices.

II. PROPOSED SYSTEM

2.1 Block Diagram

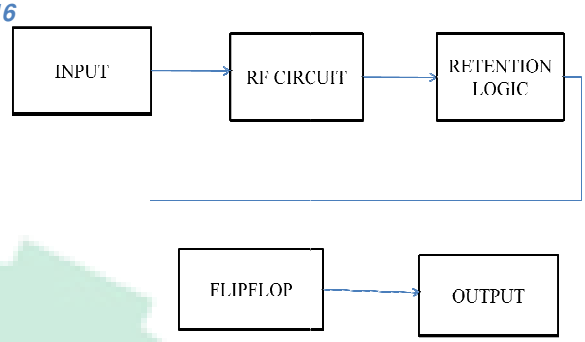

Figure 2.1 Block diagram

2.2 Simple set-reset latches SR NOR latch

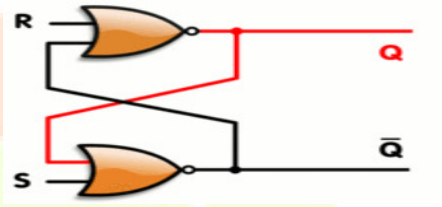

Fig: 2.2 SR NOR latch

A SR latch, constructed from a pair of cross-coupled NOR gates (an animated picture). Red and black mean logical '1' and '0', respectively.

When using static gates as building blocks, the most fundamental latch is the simple SR latch, where S and R stand for set and reset. It can be constructed from a pair of cross-coupled NOR logic gates. The stored bit is present on the output marked Q.

While the S and R inputs are both low, feedback maintains the Q and Q outputs in a constant state, with Q the complement of Q. If S (Set) is pulsed high while R (Reset) is held low, then the Q output is forced high, and stays high when S returns to low; similarly, if R is pulsed high while S is held low, then the Q output is forced low, and stays low when R returns to low.

2.3 SR NAND latch

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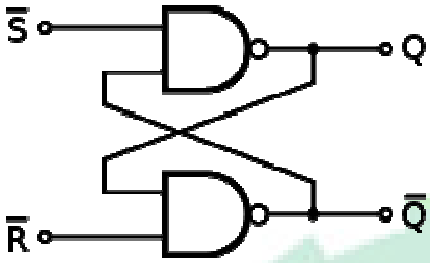

Fig 2.3: An SR latch

This is an alternate model of the simple SR latch which is built with NAND logic gates. *Set* and *reset* now become active low signals, denoted S and R respectively. Otherwise, operation is identical to that of the SR latch.

2.4 Gated latches and conditional transparency

Latches are designed to be transparent. That is, input signal changes cause immediate changes in output; when several transparent latches follow each other, using the same enable signal, signals can propagate through all of them at once. Alternatively, additional logic can be added to a simple transparent latch to make it non-transparent or opaque when another input (an "enable" input) is not asserted. By following a transparent-high latch with a transparent-low (or opaque-high) latch, a master–slave flip-flop is implemented.

2.5 Gated SR latch

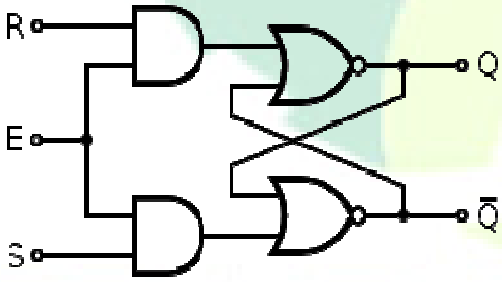

Fig: 2.4 Gated SR latch

A gated SR latch circuit diagram neither constructed from NOR gates. A synchronous SR latch (sometimes clocked SR flip-flop) can be made by adding a second level of NAND gates to the inverted SR latch (or a second level of AND gates to the direct SR latch). The extra NAND gates further invert the inputs so the simple SR latch becomes a gated SR latch (and a simple SR latch would transform into a gated SR latch with inverted enable).

2.6 Zig Bee

Zigbee is a low-cost, low-power, wireless mesh network standard targeted at wide development of long battery life devices in wireless control and monitoring applications. Zigbee devices have low latency, which further reduces average current. ZigBee chips are typically integrated with radios and with microcontrollers that have between 60-256 KB flash memory. ZigBee operates in the industrial, scientific and medical radio bands: 2.4 GHz in most jurisdictions worldwide; 784 MHz in China, 868 MHz in Europe and 915 MHz in the USA and Australia. Data rates vary from 20 kbit/s (868 MHz band) to 250 kbit/s (2.4 GHz band).

The ZigBee network layer natively supports both star and tree networks, and generic mesh networking. Every network must have one coordinator device, tasked with its creation, the control of its parameters and basic maintenance. Within star networks, the coordinator must be the central node. Both trees and meshes allow the use of Zig Bee routers to extend communication at the network level.

III. RESULTS AND DISCUSSION

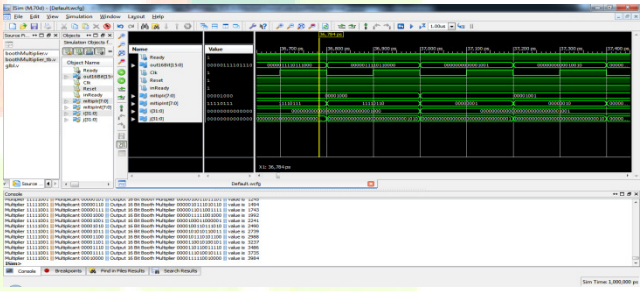

Fig: 2.5 Operand pre computation and format conversion

The multiplier receives and outputs the data with binary representation and uses only one-level carry-save adder (CSA) to avoid the carry propagation at each addition operation. The proposed multiplier receives and outputs the data with binary representation and uses only one-level carry-save adder (CSA) to avoid the carry propagation at each addition operation.

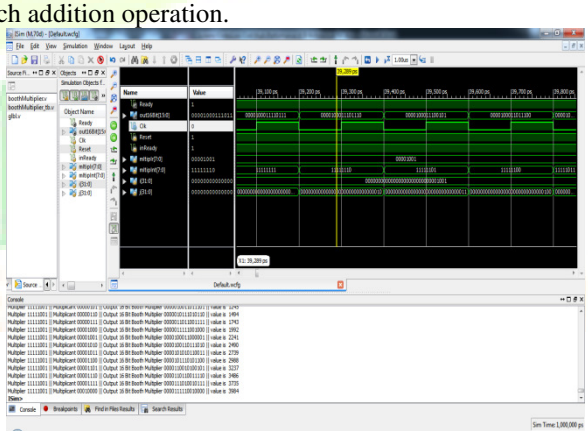

Fig: 2.6 CLK cycle process

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This CSA is also used to perform operand pre computation and format conversion from the carry save format to the binary representation. This CSA is also used to perform operand precomputation and format conversion from the carrysave format to the binary representation, leading to a low hardware cost and short critical path delay at the expense of extra clock cycles for completing one modular multiplication.

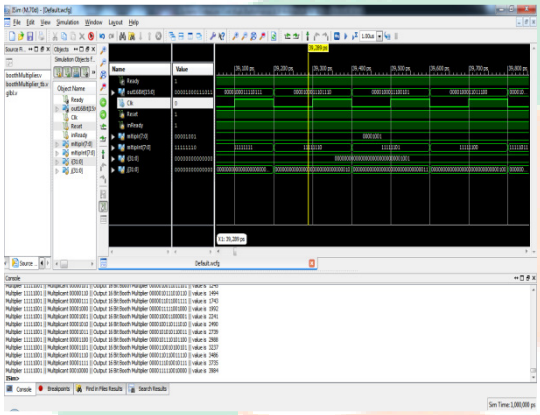

Fig: 2.7 Long carry propagation for large operands in binary

Reduce the extra clock cycles for operand pre computation and format conversion by half one full-adder or two serial half-adders.As a result, it can be easily implemented into VLSI circuits to speed up the encryption/decryption process. However, the three-operand addition in the iteration loop of Montgomery's algorithm as requires long carry propagation for large operands in binary representation.

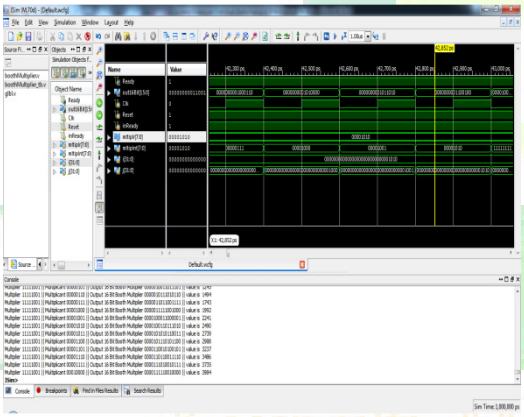

Fig: 2.8 MM Operation Measured

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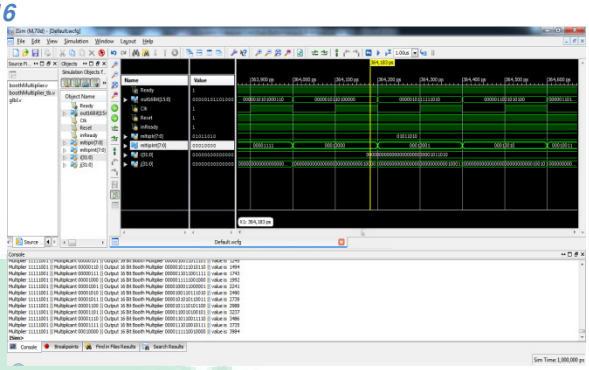

Fig: 2.9 High Performance MMM

Montgomery modular multiplier can achieve higher performance and significant area–time product improvement when compared with previous designs.

IV. CONCLUSION

FCS-based multipliers maintain the input and output operands of the Montgomery MM in the carry-save format to escape from the format conversion, leading to fewer clock cycles but larger area than SCS-based multiplier. To enhance the performance of Montgomery MM while maintaining the low hardware complexity, this paper has modified the SCS-based Montgomery multiplication algorithm and proposed a low-cost and high-performance Montgomery modular multiplier. The proposed multiplier used one-level CCSA architecture and skipped the unnecessary carry-save addition operations to largely reduce the critical path delay and required clock cycles for completing one MM operation. Experimental results showed that the proposed approaches are indeed capable of enhancing the performance of radix-2CSA-based Montgomery multiplier while maintaining low hardware complexity.

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