

# Improving Reliability of Digital Filters against MCUs Using Reduced Code Redundancies

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**Abstract**—The issue of soft errors is an important emerging concern in the design and implementation of signal processing and communication systems. It is necessary to protect data using some soft error mitigation techniques. There are so many techniques have been used including Error Correction Codes (ECC), specialized manufacturing processes, circuit level design techniques and modular redundancy. But most techniques do not efficiently protect system against Multiple Cell Upsets (MCUs) and they have complex architectures that incur large area, require more redundant bits. Here ECC is employed to protect data of digital filter which is a commonly used signal processing circuit. The proposed technique is based on Modified Decimal Matrix Code (MDMC) and this paper describes how it improves reliability of digital filters. It uses Encoder Reuse Technique (ERT) for minimizing area of extra circuits. Also it reuses Filter for Syndrome calculation which greatly reduces area overhead. MDMC is implemented in verilog, simulated using Xilinx ISE simulator and results are obtained. The proposed technique is compared with Hamming code, checksum and conventional DMC. This proves that the proposed technique requires less number of redundant bits and MDMC outperforms the other three techniques. Future work will consider applying this technique to parallel filters that they have same input signal but different impulse responses.

**Keywords** – Hamming Code, Reliability, Digital Filters, MCUs.

## I. INTRODUCTION

Nowadays as CMOS technology scales down to nanoscale this makes the system vulnerable to soft errors as described by Robert Baumann [11]. These errors are transient errors caused by the radiation particles hits the device and change the logical state of the memory cells temporarily. A wide range of techniques has been used to protect systems

against soft errors including error correction codes, specialized manufacturing processes, circuit level

design techniques and modular redundancy [1]. The effect introduced by the soft errors may be single error or single cell upset (SCU) and burst error or Multiple Cell Upset (MCU) [4]. Hence the signal processing and communication systems can be made error free with the application of protection techniques. For example, Bose-chaudhuri-hocquenghem codes, Reed-Solomon codes have been used to deal with burst errors in memories. But the main drawback of these codes is, they require more area, power and delay overhead, also they use complex encoding and decoding architectures. The MCUs can be avoided by the combination of Error Correction Code (ECC) and the interleaving technique [5], MCUs may still be problematic in high performance devices such as content addressable memories (CAMs) used in network processors and routers. The scrubbing technique has also been used to avoid temporal double-bit error. Scrubbing involves reading each part of the cache that are protected by Single Error Correcting (SEC)-ECC and recomputed the ECC after correcting any latent single bit errors and writing back the corrected bits. But the main issue in scrubbing of the caches is that it requires extra overhead in terms of software and/or hardware. Since the scrubbing have to access every block in a large cache. Built-in current sensors (BICS) are proposed to assist with single-error correction and double-error detection codes to provide protection against MCU. However, this technique can only correct two errors in a word.

More recently, in , 2-D matrix codes (MCs) are proposed to efficiently correct MCUs per word

with a low decoding delay, in which one word is divided into multiple rows and multiple columns in logical. The bits per row are protected by Hamming code, while parity code is added in each column. For the MC [6] based on Hamming, when two errors are detected by Hamming, the vertical syndrome bits are activated so that these two errors can be corrected. As a result, MC is capable of correcting only two errors in all cases. In an approach that combines decimal algorithm with Hamming code has been conceived to be applied at software level. It uses addition of integer values to detect and correct soft errors. The results obtained have shown that this approach have a lower delay overhead over other codes.

Some commonly used techniques are modular redundancy where the circuit to be protected is replicated N times and extra logic is added to detect and correct errors. If N equals to two, then the technique is known as Dual Modular Redundancy (DMR). In DMR [2] the outputs of two modules are compared, if they differ an error is detected. Conventional DMR does not provide error Correction. In the same way, if N equals to three, then the Technique is known as Triple Modular Redundancy (TMR). TMR provides error detection as well as correction. Duplication and comparison or DMR and TMR are the most commonly used in logic parts. But they introduce excessive area and power penalty, making them unacceptable in most designs.

Signal processing circuits are used in many applications like communications, data storage, audio processing, and video processing. Some of the devices involved in signal processing are filters, samplers, signal compressors and digital signal processors. In that case, there are two main types of digital filter, they are recursive and non-recursive filters. They are referred as Infinite Impulse Response (IIR) and Finite Impulse Response (FIR), respectively. The FIR filters are widely used as they have good stability and they can be easily designed to match a given response. This paper describes efficient coding techniques for improving reliability of generic FIR filter.

In the rest of the paper, first the Background and its related work using ECC are described. Second, the proposed coding Technique MDMC is presented. Third, the results are analyzed, compared to the existing ECC techniques. Fourth, concluded from the above work.

## II. BACKGROUND AND RELATED WORK

When signal is sent through some transmission media it is subjected to attenuation, distortion and noise, as a result some of the bits of the data or signal gets corrupted i.e., it leads to some error in sending data. To achieve reliable communication through the unreliable media, some mechanisms have been devised to detect and correct those errors during transmission.

### A. Error Detecting and Error Correcting Codes

The simplest and cost effective solution for protecting a system is to add a parity bit/redundancy to each word in the system memory. During each write operation, a parity generator computes the parity bit of the data to be written as illustrated in fig 1. The data together with the computed parity bit are written in the memory. If a particle strike changes the data word, it incurs an error during the read operation. While reading data, the parity bits are recomputed for error detection [8]. Error correction is done by error recovery technique.

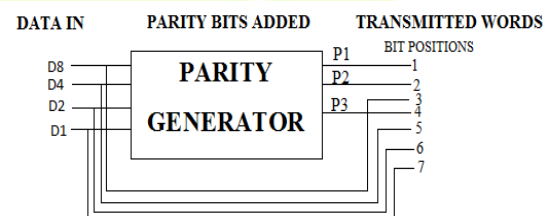


Figure 1: Parity Generator.

### FIR Filter Implementation:

A FIR filter implements the following equation:

$$y[n] = \sum_{i=0}^{N-1} x[n-i] \cdot h[i] \quad (1)$$

Where  $h[i]$  is the impulse response given to filter that operates on the input signal  $x[n]$ . The impulse response can be infinite or be non-zero for a finite number of samples. In the first case the filter is an Infinite Impulse Response (IIR) filter and in the second a Finite Impulse Response (FIR) filters [10]. As mentioned earlier that this paper describes ECC for generic FIR filter as given in fig 2. In this



structure, D flip-flop can be used as the delay for a 4 tap filter. element and the impulse responses named as a (4:0)

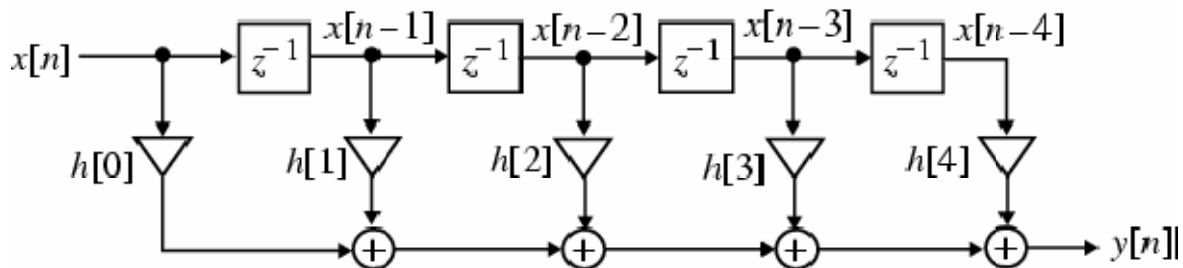


Figure 2: Direct form FIR filter structure

The existing technique of this paper utilizes hamming code and checksum algorithm to protect generic FIR filter as given above. Hamming codes are linear block codes and also Forward Error Correction Code that can correct single error and detect up to double bit errors. The minimum distance of the code should be equal to 3. The hamming codes have the following parameters [3]:

$$n = 2^m - 1 \quad (2)$$

$$k = n - m \quad (3)$$

$$d_{\min} = 3$$

Where  $n$  is the code size,  $m$  is the number of parity bits/ check bits,  $k$  is the number of information bits and  $d_{\min}$  is the minimum distance of the code. The position of parity bits are placed in such a way that it can give different error results for different incorrect bits. Some possible values of the above parameters are illustrated in Table I. Thus the parity bits are calculated using parity generator and decoder calculates a syndrome value. If the syndrome value is zero, it means there is no error and the non zero syndrome value indicates the presence of error. Basic Hamming codes are perfect. For example, H (7, 4) has 3 parity bits and the syndrome has also 3 bits. In this way, there are 8 possible values for the syndrome.

TABLE I.

HAMMING CODE PARAMETERS

k	n
4	7

11	15
26	31
57	63
120	127
247	255
503	511

The zero syndromes are assigned to the “no error” condition, and the remaining values are assigned to the bits of the encoded word one-to-one. Based on this idea, three redundant modules for parallel FIR filter are utilized. Here each filter is considered as a bit. Hence for four parallel FIR filters requires three redundant FIR filters to act as redundant modules as in fig 3.

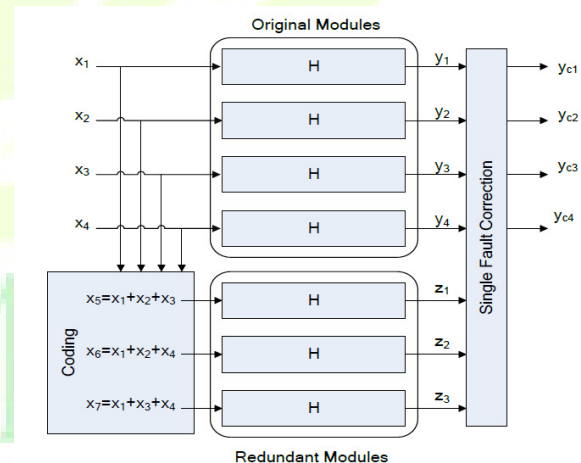


Figure 3: ECC based scheme for four filters and a Hamming code.

As it can be seen from the results obtained, the main drawback of Hamming codes is that a double error

generates a syndrome assigned to a single error correction, leading to a wrong correction and, consequently, to a wrong decoding.

### B. Checksum Implementation

Checksum is used for checking data integrity while transmission or storage of data. In checksum, at the transmitter end the whole data is divided and added with the consecutive words, hence it produces checksum output. At the receiver end, the checksum value is recomputed and compared with the previous output. If MCUs are detected it can be corrected thereby. Here checksum algorithm is used to check for error while transmitting through FIR filter. This implementation is outlined in fig 4.

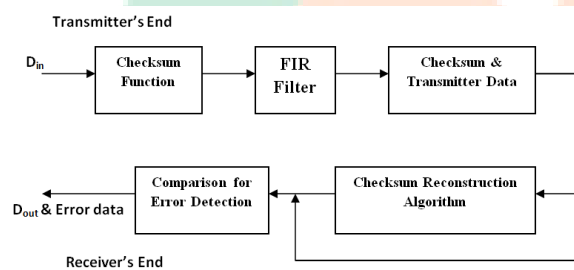


Figure 4: Outline of Checksum Implementation.

This checksum algorithm is implemented for 32-bit data using FIR filter [9]. At the transmitter's end, the 32-bit data is divided into k segments (4-segments) each of m bits (8-bits). The segments are added using one's complement arithmetic to get the checksum. These segments are sent along with the checksum to the receiver's end through FIR filter.

At the receiver's end, all the received segments are added using one's complement arithmetic to get the reconstructed checksum output. This output is compared with the checksum computed at the transmitter's end to check for errors. If the results are not equal then the error is detected and thereby correction can be made.

### III. MODIFIED DECIMAL MATRIX CODE (MDMC) TECHNIQUE

The proposed technique for fault free generic (FIR) filter is outlined in fig 5. [7]. During the encoding (write) operation information bits D are fed to the MDMC encoder. The redundant bits X are

obtained from the MDMC encoder. If MCUs occur in filter, it can be detected by recomputed the redundant bits. Then in the error locator, the position of the error can be obtained.

### A. MDMC Encoder

MDMC is based on divide symbol and arrange matrix ideas. Also encoder reuse technique (ERT) is employed to reduce area overhead. It should be noted that above ideas are implemented in logical instead of in physical. Divide mechanism as in fig 6. is based on dividing the N-bit word into k symbols of m bits ( $N = k \times m$ ) and these are arranged in a  $k_1 \times k_2$  2-D matrix where  $k_1 \times k_2$  represent the number of rows and columns respectively. Then the redundant bits (X) are calculated by performing decimal integer additions of selected symbols per row. The above ideas are implemented in a 32-bit word and the results are obtained.

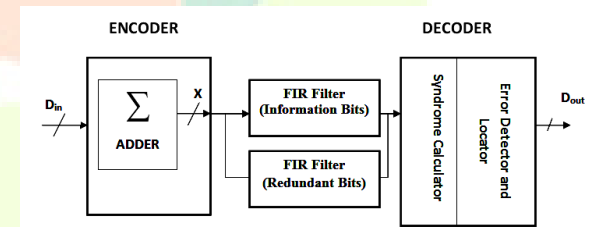


Figure 5: Outline of Modified Decimal Matrix Code.

Here 32-bit ( $D_0 - D_{31}$ ) information bits are divided into 8 symbols ( $2 \times 4$ ) each of 4 bits.  $k_1 = 2$ ,  $k_2 = 4$  have been chosen simultaneously. It is to be noted that the number of redundant bits vary for different k and m values are chosen. The redundant bits X can be obtained as follows,

$$X_1 = D_3 D_2 D_1 D_0 + D_{11} D_{10} D_9 D_8 \quad (4)$$

$$X_2 = D_{27} D_{26} D_{25} D_{24} + D_{19} D_{18} D_{17} D_{16} \quad (5)$$

$$X_3 = D_{15} D_{14} D_{13} D_{12} + D_7 D_6 D_5 D_4 \quad (6)$$

$$X_4 = D_{31} D_{30} D_{29} D_{28} + D_{23} D_{22} D_{21} D_{20} \quad (7)$$

Hence the above computation takes place in a 32-bit MDMC encoder structure using multibit adders as in Fig 7.

### B. MDMC Decoder



To obtain a word being corrected the decoding process is required. The copy of information bits and redundant bits are sent through FIR filter and encoder (ERT) to be recomputed. These are said to as syndrome bits ( $y_1, y_2, y_3 \dots y_{12}$ ) as given in fig 8. Then these bits are compared with the recomputed syndrome bits  $z_1, z_2, z_3$  and  $z_4$  to detect and locate the errors.

For example:

$$y[n] = \sum_{i=0}^4 x[n-i] \cdot h[i] \quad (8)$$

$D_{15}D_{14}D_{13}D_{12}$	$D_{11}D_{10}D_9D_8$	$D_7D_6D_5D_4$	$D_3D_2D_1D_0$	$X_3$	$X_1$
$D_{31}D_{30}D_{29}D_{28}$	$D_{27}D_{26}D_{25}D_{24}$	$D_{23}D_{22}D_{21}D_{20}$	$D_{19}D_{18}D_{17}D_{16}$	$X_4$	$X_2$

Figure 6: Divide mechanism on 32-bit MDMC Encoder.

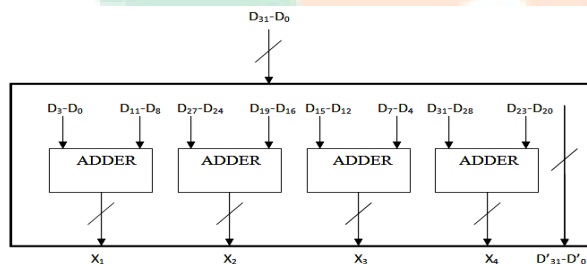


Figure 7: 32-bit MDMC encoder structure.

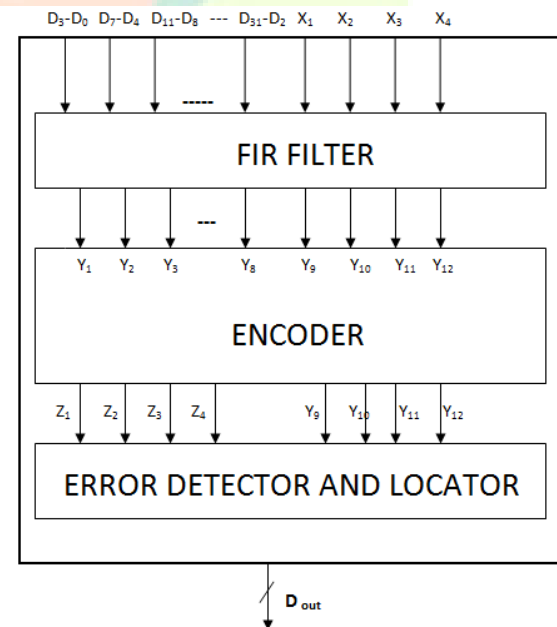


Figure 8: 32-bit MDMC Decoder structure.

These recomputed syndrome bits are again added using Encoder Reuse Technique (ERT) and named as  $z_1, z_2, z_3, z_4$ . These bits are compared with the recalculated bits  $y_9, y_{10}, y_{11}, y_{12}$ . Error bits ( $e_1, e_2, e_3$ ,

$e_4$  ) are obtained by comparing the above computed bits, thereby producing the output  $D_{out}$ .

$$e_1 = z_1 == y_9 \quad (9)$$

$$e_2 = z_2 == y_{10} \quad (10)$$

$$e_3 = z_3 == y_{11} \quad (11)$$

$$e_4 = z_4 == y_{12} \quad (12)$$

In the proposed technique MDMC, the circuit area is minimized by reusing its encoder. This is called Encoder Reuse Technique (ERT). The ERT can reduce area overhead and it should be noted that FIR filter is also reused for syndrome calculation. Hence the whole circuit area can be reduced.

#### IV. RESULT ANALYSIS

In this section, the proposed methods has been implemented in verilog, simulated with Xilinx and tested for functionality by giving various inputs.

The area, power and delay also have been obtained. The requirement of redundant bits of other codes has been compared with MDMC Technique as given in Table II. Coding Efficiency ( $\beta$ ) [7] is used to obtain the area overheads given as follows;

$$\beta = \frac{\text{Redundant Bits}}{\text{Information Bits} + \text{Redundant Bits}} \quad (8)$$

From the above redundant bits analysis, MDMC provides higher coding efficiency compared to other codes but reduced from Conventional DMC technique. But their requirements of redundant bits have been reduced. Hamming code requires very less no. of redundant bits but its coding efficiency is less, since it can detect double error and corrects single error only. Checksum is between the other codes but still it can locate and correct single and multiple errors.

TABLE II.

REDUNDANT BITS

Method	No. of Information Bits	No. of Redundant Bits	$\beta$	ECC Capability
Modified DMC	32	16	33.3%	ECC up to 5 bits
DMC	32	36	52.9%	$k = 2 \times 4, m = 2$
Checksum	32	8	20%	Locates and corrects single and Multiple Cell upsets
Hamming code	32	7	17.9%	Double error detection and Single error correction

and Checksum) and their comparison is also presented. The requirement of redundant bits is greatly reduced when compared to the conventional techniques. Therefore, the proposed technique can be useful to implement fault free FIR filter. Future work will consider applying this technique to parallel filters that they have same input signal but different impulse responses.

#### V. CONCLUSION

The Modified Decimal Matrix Code (MDMC) using generic FIR filter for improving reliability of the filter has been presented in this paper. The proposed technique uses encoder Reuse Technique (ERT), as it helps in reducing area overhead of the circuit. The coding of this technique has been implemented in verilog and also verified with various input combinations. This MDMC outperforms the other techniques (Hamming code

#### ACKNOWLEDGMENT

I express my sincere gratitude to my guide Mr.T.Karthik, Assistant Professor, Department of

ECE for guiding my research work throughout the process and I extend my thanks to Karpagam college of Engineering.

#### REFERENCES

[1] M. Nicolaidis, "Design for soft error mitigation," IEEE Trans. Device Mater. Rel., vol. 5, no. 3, pp. 405–418, Sep. 2005.

[2] Pedro Reviriego, Chris J. Bleakley, And Juan Antonio Maestro, "Structural DMR: A Technique For Implementation Of Soft-Error-Tolerant Fir Filters",

IEEE Transactions On Circuits And Systems—II: Express Briefs, Vol. 58, No. 8, August 2011.

[3] R. W. Hamming, "Error detecting and error correcting codes," Bell Syst. Tech. J., vol. 29, no. 2, pp. 147–160, Apr. 1950.

[4] P. Reviriego, J. A. Maestro, and C. Cervantes, "Reliability analysis of memories suffering multiple bit upsets," IEEE Trans. Device Mater. Rel., vol. 7, no. 4, pp. 592–601, Dec. 2007.

[5] S. Baeg, S. Wen, and R. Wong, "SRAM interleaving distance selection with a soft error failure model," IEEE Trans. Nucl. Sci., vol. 56, no. 4, pp. 2111–2118, Aug. 2009, Part2.

[6] A. Sanchez-Macian, P. Reviriego, and J.A. Maestro, "Enhanced Detection of Double and Triple Adjacent Errors in Hamming Codes through Selective Bit Placement," IEEE Transactions on Device and Materials Reliability, vol. 12(2), June.2012, pp.357-362.

[7] Jing Guo, Liyi Xiao, Member, Ieee, Zhigang Mao, Member, Ieee, And Qiang Zhao, "Enhanced Memory Reliability Against Multiple Cell Upsets Using Decimal Matrix Code", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 1, January 2014.

[8] Zhen Gao, Pedro Reviriego, Zhan Xu, Xin Su, Jing Wang and Juan Antonio Maestro, "Efficient Coding Schemes for Fault Tolerant Parallel Filters".

[9] Zagar, B. Dept. of Electr. Eng. & Comput. Sci., California Univ., Davis, CA, USA ,Redinbo, R., "Watchdog parity channels for digital filter protection".

[10] Shih-Fu Liu, Pedro Reviriego and Juan Antonio Maestro, " Fault Tolerant FIR filters using Hamming Codes", RADECS 2009 Proceedings.

[11] Robert Baumann, Texas Instruments, "Soft Errors in Advanced Computer Systems", IEEE Design & Test of Computers, 2005.