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Efficient Implementation of ADMA on Bus Based SoC

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Abstract-- Power models are at the heart of high level estimation methods for industrial, efficient evaluation of system on-chip bus protocol termed as MSBUS-DMA. The efficiency of DMA had less throughput, performance level also less in while transferring data during block transfer mode. The main issue of DMA extra hardware cost and extra code size, and complexity of the software are high. In this paper to improve bandwidth, low power, low cost and in order to reduce complexity advanced direct memory access controller (ADMA) is proposed methodology. To estimate bus performance in various analytical models including area, power, entire performance level, speed of data while transmitting, time consumption, bandwidth as achieves high performance ADMA–ID ASSIGNMENT technique based on bus based system on-chip.

Index Terms: DMA Controller, SoC ADMA-ID assignment, performance estimation.

I. INTRODUCTION

In system-based data acquisition applications, data transmitting or receiving through computer I/O devices must often be managed at high speeds or in large quantities. The three primary data transfer mechanisms for computer-based data acquisition are polling, interrupts (also known as programmed I/O), and direct memory access (DMA).Today, the reduced interface difficulty and low energy on-chip bus termed as receiving more attention. Bus protocol is similar to communication link. Bus protocol can transfer the data through AMBA Bus(advanced microcontroller bus architecture) .In industry applicants, the most Advanced High Performance Bus(AHB),and Advanced extensible Interface(AXI) from ARM holding. AMBA Bus is a type of linear bus; all of these following buses transfer data linearly; however in some applications such as digital image processing, wireless communication, and computer vision is based on data neighbours, adjacency, regions, and boundaries and block data load and storage. Advanced bus structures such as multi-bus and multiple layers of architecture, the bandwidth, efficiency, can be improved when most of communication occurs in same bus level or the same bus layer. However, a greater number of wires and interior logic such as multiplexers for different layer data conversions, and buffers or first-in–first-outs (FIFOs) for data flow control are necessary, which are more costly in terms of both area and energy consumptions.

To get better of this above limitation, a low cost and low energy bus named master-slave bus (MSBUS). In this paper to improve bandwidth, low power, low cost and in order to reduce complexity MSBUS advanced direct memory access controller (ADMA) is proposed methodology**.** To evaluate the bus performance, we can improve the efficiency level as compare to MSBUS-DMA.

Here master bus can support several slaves is possible.No routing problem can occur by using MSBUS-ADMA.

The remainder of this paper is organised as follows. In Section II Existing technique of DMA, In Section III introduces the Routing technique estimation, Section IV Overall procedure of proposed technique,Section V MSBUS protocol based on SOC. Finally Section VI, ID ASSIGNMENT MODULE ,Section VII Result anlysis ,Section VIII conclude this paper.

II. EXISTING TECHNIQUE OF DMA

A direct memory access (DMA) is an operation in which data is copied (transported) from one resource to another resource in a computer system without the involvement of the CPU. The task of a DMA-controller (DMAC) is to execute the copy operation of data from one resource location to another. The copy of data can be performed from: I/O device to memory, memory to I/O device. The DMA channel source address register (SRC) contains address for next read transfer. The DMA channel destination address register (DST) contains address for next write transfer. Source and destination addresses can be incremented or decremented by the element size after each transfer. DMA has several advantages over polling and interrupts. DMA is fast because a dedicated piece of hardware transfers data from one computer location to another and only one or two bus read/write cycles are required per piece of data transferred. In addition, DMA is usually required to achieve maximum data transfer speed, and thus is useful for high speed data acquisition devices. DMA also minimizes latency in servicing a data acquisition device because the dedicated hardware responds more quickly than interrupts, and transfer time is short. Minimizing latency reduces the amount of temporary storage (memory) required on an I/O device. DMA also off-loads the processor, which means the processor does not have to execute any instructions to transfer data.

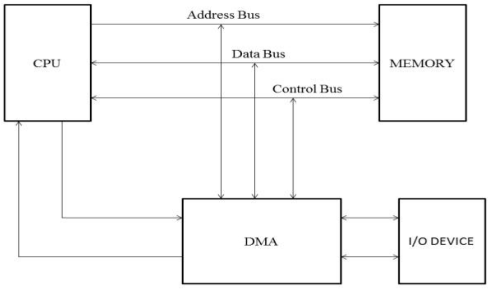

Fig.1. Block diagram of DMA.

III.ROUTING TECHNIQUE

Route is one of the way to send data in correct destination. For example ,4X4 master and slave bus are taken .M1,M2,M3,M4 for 4 inputs master side .S1,S2,S3,S4 for 4 outputs slave side.As centre bus layer can be placed ,while inside the bus address can route in both sides i.e iput and output side .

With the help of address route master M1 data reached particular data in correct slaves(S1,S2,S3,S4). If one layer to another layer can transfer data in very large module ,in between the layers we connect local ports.Local ports is one kind of path.

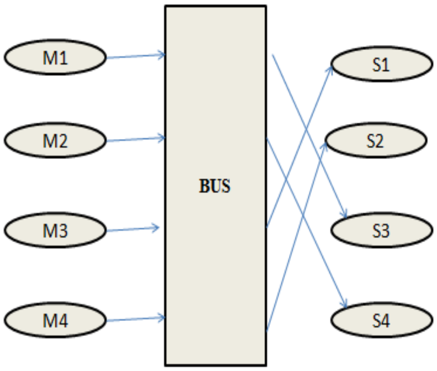

FIG 4. 4X4 MSBUS DATA TRANSFER

IV. PROPOSED TECHNIQUE

Direct Memory Access controller (DMAC) is an important component of SoC architecture and Direct Memory Access (DMA) is an important technique to increase data transfer rate and MPU (microprocessor unit) efficiency in SoC system. There are a few of on-chip bus standards; AMBA (Advance Microcontroller Bus Architecture) has become popular industry-standard on-chip bus architecture. The design of DMAC is compliance to the AMBA specification for easy integration into SoC.

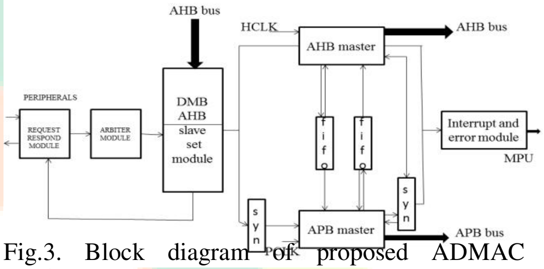

Fig.3. Block diagram of proposed ADMAC architecture.

Firstly, MPU programs the parameter set associated with the channel by DMA ARB Slave interface. AHB arbiter tends to be bus arbiter insures that only one bus master at time is allowed to initiated data transfer. Advanced DMA controller technique used to save time for reduced the complexity. AHB is used for high speed and frequency operation and also supports multiple masters. AHB master only one bus master is allowed to actively use the bus at any one time. AHB slave accepts the data while receive the data from master bus and sends the acknowledgement to AHB master. FIFO is used to corresponding to each channel. FIFO supports byte by byte transfer of data. Data transferred through user defined size FIFO. Interrupt used to give confirmation of it. Balances performance with cost, efficient, and implementation the features are five programmable address modes, byte or word support for data transfer, software triggered transfer. And interrupt signal and error signal could be masked by setting control resister in parameter set.

IV. MSBUS PROTOCOL

Master-slave bus is serial peripheral interface. Bus organisation has control lines and data lines. Control lines are termed as control bus, data lines is termed as data bus. Since control lines have signal request and acknowledge, data lines have to carry the information between source and destination .MBUS stands for master bus with a single master-the microprocessor, and SBUS stands for slave bus with single slave-the memory controller. MBUS defines the single transfer mode for minimal power consumption and reduced

WORK	POWER	TIMING
EXISTING METHOD ROUTING	0.171w	1.247s
PROPOSED METHOD ADMA-ID	0.168w	0.696s

interface complexity. MSBUS protocol is very desirable for small scale embedded systems with requirements of a low cost interface and high energy efficiency. MBUS protocol to detect command errors. If current response is a timeout, the command is indicated as "error" and must be "retried" or "discarded" by the master.

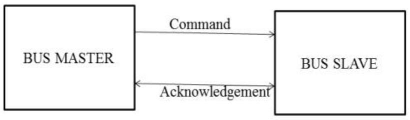

Fig.4.MSBUS PROTOCOL

Here master bus can support several slaves is possible.No routing problem can occur by using MSBUS-ADMA.

VI.ID ASSIGNMENT MODULE.

To overcome the routing problem we can move to ID TAGS i.e. each and every source have individual destination .In case huge number of master and slave bus data transaction, errors had occur. However data transferring time, power, devices speed all are collapsed

So we can go for ID TAGS.By assigning ID tags for each and every masters and slaves They can easily identified which location had an errors that only we go ID ASSIGNMENT TAGS.

For huge number of data transfer means i.e 64 bits ,we go to spilt 8 bit for packets,and another 8 bits for address locations. Hence 8 bits of packets include the ID tags number.ID tags can be separate into three characters.

I) HEADER
II) TAIL
III) BODY

For header is used to allocate address,tail is used to COUNTER ID value,and atlast body is used to data transferrimg mode.

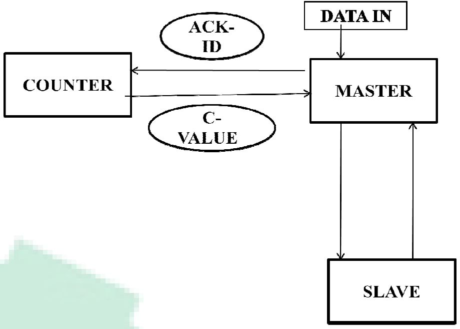

Fig.5.ID ASSIGNMENT MODULE

From the above figure data transfer in one side of module .For example 8 bit data as an input of master ,and 3 bit of data comes under from counter. The counter value of each bitwidth have assigned ID TAG NUMBER.

Table.1
Data and ID assignment location

2^3=8
8 BIT DATA is an input.

D 0	D 1	D 2	D 3	D 4	D 5	D 6	D 7	I 0	I 1	I 2

The master is source address and slave is destination address,counter can count the data bit width and sends the data in master .C-VALUE refers value from counter to master side.

While counter value starts with initial bit value and it starts from '0'to'7'.

Table.2
Id assignment and counter value assigniment.

Counter value	2^3=8	ID ASSIGNMENT
0	000	1
1	001	2
2	010	3
3	011	4
4	100	5
5	101	6
6	110	7
7	111	⟷

The proposed technique of ADMA-ID ASSIGNMENT ,data input is 8 bit data is given and

CLK is set as “1”and RST value is initially “0”and after some period is set as“1”.hence the output of dataout is analysed very easy and highly improved the speed of data transfer mode.

DATAOUT=DATAIN+COUNTER VALUE.

For example , we take 110 bit value, checks the first counter value assigned .so 110=6 th place of counter value,hence in ID ASSIGNMENT 6th place occupies the value 101.So one bitwidth value moves faster,dataout is datain+101 is an output.

VII.RESULT ANALYSIS

From this above proposed technique we analysed speed of data transferring from source to destination ,and power &time period,etc.

VIII. CONCLUSION

We proposed ADMA-MSBUS achives a high-performance bus with reduced interface complexity, minimal power consumption, and high bandwidth. The coding of this technique has been implemented in verilog language and also verified with various applications.DMA-MSBUS has routing problem can be solved by proposed technique ADMA-ID ASSIGNMENT and compared the area, power and timing values. This technique is very suitable for huge number data transferring method. Advantage of high speed transfer rate and efficient is much suitable to various application fields, such as multimedia processing wireless communication ,etc.Hence we done the work with proposed technique of ADMA-ID ASSIGNMENT.

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