



# Design of MX-CQCA Based Ripple Carry Adder Using QCA Designer

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**Abstract**— Quantum dots cellular automata (QCA) are novel devices which are promising in the era of nanoscale computing. This paper presents the design of MX-CQCA based ripple carry adder (RCA). We first compare the design of traditional full adder based ripple carry adder and MX-CQCA based ripple carry adder in HDL environment. Also, the QCA layout of MX-CQCA based ripple carry adder is generated using the QCADesigner software. Our experimental results show that the MX-CQCA based ripple carry adder consumes less power compared to Fredkin gate based ripple carry

**Index Terms**— Quantum dots cellular automata, Nano technology, ripple carry adder, QCADesigner software.

## I. INTRODUCTION

QCA is one of the emerging nanotechnologies in which it is possible to implement reversible logic gates. Quantum-dot cellular automata (QCA) are locally interconnected cellular-automata-like arrays of nanostructures (quantum dots). Here interconnections are given by the physical interactions. QCA makes it possible to achieve circuit densities and clock frequencies beyond the limits of existing CMOS technology. In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell. Thus, when the bit is flipped from 1 to 0 there is no actual discharging of the capacitor as in conventional CMOS. Hence, QCA does not have to dissipate all its signal energy during transition. Further, propagation of the polarization from one cell to another is because of interaction of the electrons in adjacent QCA cells. As there is no movement of electrons from one QCA cell to the other, there is no current flow.

QCA makes it possible to achieve circuit densities and clock frequencies beyond the limits of existing CMOS technology [1, 2]. In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell as illustrated in Figure. 1. Thus, when the bit is flipped from 1 to 0 there is no actual discharging of the capacitor as in conventional CMOS. Hence, QCA does not have to dissipate all its signal energy during transition. Therefore, QCA has significant advantage compared to CMOS technology in terms of power dissipation.

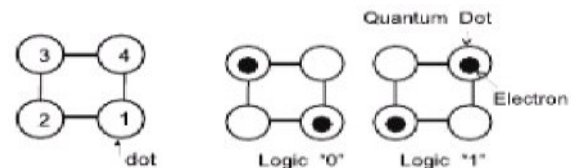


Fig. 1 (a) QCA (b) QCA cell logic 0 and logic 1

Many electronic computing circuits have been proposed using QCA technology. In this paper we review the design of Fredkin gate and MX-CQCA gate and an attempt is made to design the ripple carry adder circuit using MX-CQCA. The rest of the paper is organized as follows. Section II describes the design of Fredkin gate and MX-QCA. Section III explains the design of ripple carry adder using MX-CQCA. Section IV presents the layout design using QCADesigner software. Section V summarizes the experimental results and section VI concludes the paper.

## II. DESIGN OF FREDKIN GATE AND MX-CQCA

### A. Fredkin Gate

The Fredkin gate is a commonly used reversible conservative logic gate, first proposed by Fredkin and Toffoli in [3]. The Fredkin gate is described as a mapping (A, B, C) to (P = A, Q = A'B + AC, R = AB + A'C), where A, B, C are the inputs and P, Q, R are the outputs, respectively as shown in Figure 2. The truth table of the Fredkin gate [4] is shown in Table 1, and it demonstrates that Fredkin gate, is reversible and conservative in nature. It has unique input and output mapping and also has the same number of 1s in the outputs as in the inputs.



Fig.2. Fredkin gate



TABLE I: TRUTH TABLE OF FREDKIN GATE

| Inputs |   |   | Outputs |   |   |
|--------|---|---|---------|---|---|
| A      | B | C | P       | Q | R |
| 0      | 0 | 0 | 0       | 0 | 0 |
| 0      | 0 | 1 | 0       | 0 | 1 |
| 0      | 1 | 0 | 0       | 1 | 0 |
| 0      | 1 | 1 | 0       | 1 | 1 |
| 1      | 0 | 0 | 1       | 0 | 0 |
| 1      | 0 | 1 | 1       | 1 | 0 |
| 1      | 1 | 0 | 1       | 0 | 1 |
| 1      | 1 | 1 | 1       | 1 | 1 |

### B. Multiplexer Conservative QCA Gate

Multiplexer Conservative QCA Gate is a conservative logic gate that is conservative in nature but is not reversible. It has three inputs and three outputs as shown in Figure 3. MX-CQCA has one of its outputs working as a multiplexer that will help in mapping the sequential circuits based on it, while the other two outputs work as AND and OR gates, respectively. The mapping of the inputs to outputs of the MX-CQCA is:  $P = AB$ ;  $Q = AB' + BC$ ;  $R = B + C$ , where A, B, and C are the inputs and P, Q, R are the outputs, respectively. Table 2 shows the truth table of the MX-CQCA gate. The number of 1s in the inputs is equal to the number of 1s in the outputs and hence it is conservative in nature [5].

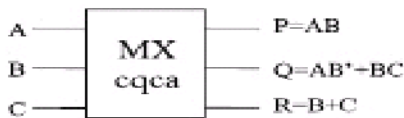


Fig. 3. MX-cqca gate

TABLE II: TRUTH TABLE OF MX-CQCA GATE

| INPUTS |   |   | OUTPUTS |   |   |
|--------|---|---|---------|---|---|
| A      | B | C | P       | Q | R |
| 0      | 0 | 0 | 0       | 0 | 0 |
| 0      | 0 | 1 | 0       | 0 | 1 |
| 0      | 1 | 0 | 0       | 0 | 1 |
| 0      | 1 | 1 | 0       | 1 | 1 |
| 1      | 0 | 0 | 0       | 1 | 0 |
| 1      | 0 | 1 | 0       | 1 | 1 |
| 1      | 1 | 0 | 1       | 0 | 1 |
| 1      | 1 | 1 | 1       | 1 | 1 |

## III. DESIGN OF RIPPLE CARRY ADDER USING MX-CQCA

### A. Full adder based RCA

The design a 4-bit adder circuit is started by designing the 1-bit full adder then connecting four 1-bit full adders to get the 4-bit adder. A one-bit full adder is a combinational circuit that forms the arithmetic sum of three bits. It consists of three inputs (A, B, Cin) and two outputs (S and Cout) as illustrated

in Figure 4(a). The Boolean expressions describing full adder are given by Equation (1) and Equation (2).

$$S = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = AB + BC_{in} + C_{in}A \quad (2)$$

The truth table of the full adder is listed in Table 3. The gate level implementation of 1-bit full adder is shown in Figure 4(b).

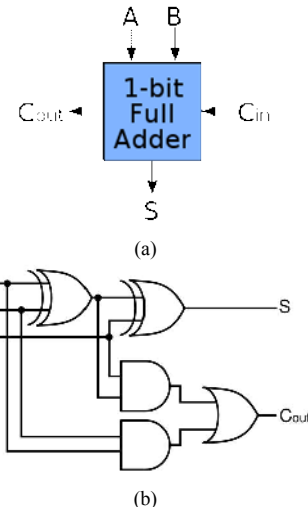


Fig. 4. (a) Schematic of 1-bit full adder (b) Gate level implementation of 1-bit full adder

TABLE III: TRUTH TABLE OF 1-BIT FULL ADDER

| A | B | Cin | S | Cout |
|---|---|-----|---|------|
| 0 | 0 | 0   | 0 | 0    |
| 0 | 0 | 1   | 1 | 0    |
| 0 | 1 | 0   | 1 | 0    |
| 0 | 1 | 1   | 0 | 1    |
| 1 | 0 | 0   | 1 | 0    |
| 1 | 0 | 1   | 0 | 1    |
| 1 | 1 | 0   | 0 | 1    |
| 1 | 1 | 1   | 1 | 1    |

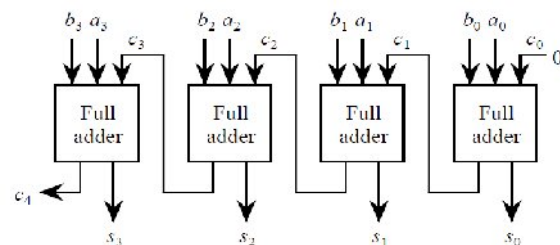


Fig.5. 4-bit ripple carry adder

The schematic of 4-bit ripple carry adder is shown in Figure 5. Initially the C0 bit is assigned to zero and a0, b0 inputs are applied to the first full adder. The Sum is taking as a LSB bit of output the carry signal is given to the next full adder input C1. In this C1 is added with a1 and b1 the sum S1 and carry c2 will be generated. The carry C2 is the input of the next full



adder. In this C2 is added with a2 and b2 the sum S2 and carry C3 will be generated. The carry C3 is the input of the next full adder. In this C3 is added with a3 and b3 the sum S3 and carry C4 will be generated.

#### B. MX-CQCA based RCA

MX-CQCA based ripple carry adder as shown Figure 6. In this design majority voters are used to produce the sum and carry output signal. Each full adder is implemented using MX-CQCA gate and they are connected similar to the full adder based RCA circuit.

#### IV. LAYOUT DESIGN USING QCADesigner SOFTWARE

QCADesigner is the product of an ongoing research effort by the Walus Group at the University of British Columbia to create a design and simulation tool for Quantum Dot Cellular Automata (QCA). This tool is still under development and is provided free of cost to the research community "as is" [6]. QCA is an emerging concept in computational nanotechnology for the realization of a computer using arrays of nano-scale QCA cells. These QCA cells are capable of performing all complex computational functions required for general-purpose computation (majority function, Inversion, and fan-out). The QCADesigner tool facilitates rapid design, layout and simulation of QCA circuits by providing powerful CAD features available in more complex circuit design tools [7].

##### A. Working Steps for QCADesigner 2.0.3:

1. Click start → QCA Designer.
2. Select Tools → Import block and select your drive and type file name with extension of .qca and click ok button.
3. Cell is a single QCA cell. Array is a number of QCA cell. Select is used to select the particular cell. Rotate is used to rotate the quantum dots.
4. By using the Cell and Array icon we are placing QCA cell in our work place based on the circuit.
5. By Setting the input/output cell first we select that cell and double click in that cell display a cell function dialogue box. In that box we are select input/output button and give a cell label name and click on ok button.
6. By setting polarization value first we are select that cell and double click in that cell display a cell function dialogue box. In that box we are select fixed polarization and give the value it is generally -1.00 or +1.00 after setting that value click on ok button.
7. After completing layout designing the layout will be simulated and the output will be verified. Select simulation → start simulation, simulation results window

will be appeared.

#### V. EXPERIMENTAL RESULTS AND DISCUSSION

##### A. Experimental setup

The design of Fredkin gate, and MX-CQCA are carried out in HDL environment with Xilinx software and the layout design is done with the QCADesigner as described in Section IV.

##### B. Results and Discussion

The QCA layout of Fredkin gate is shown in Figure 7. In this layout, A, B, C are the three inputs and P, Q, R are the three outputs. This implementation requires six majority voters. The HDL implementation and QCA layout of QCA layout are shown in Figure 8 and Figure 9 respectively. The functionality of MX-CQCA gate is given by the formula  $P=AB$ ,  $Q=AB'+BC$  and  $R=B+C$ . The Combination of input is given to A, B, and C the required outputs are obtained at P, Q, and R. In the QCA layout for MX-CQCA gate shown in Figure 9, A, B, C are the three inputs and P, Q, R are the output. Five majority voters are required for this implementation.

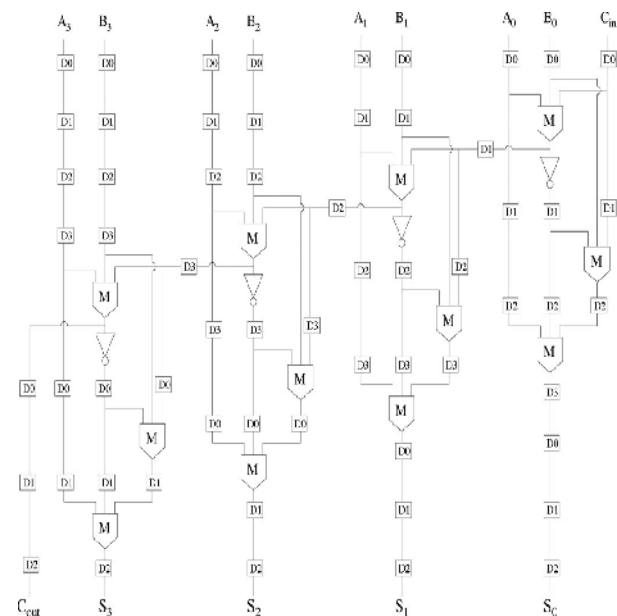


Fig. 6. Ripple Carry Adder using MX-CQCA

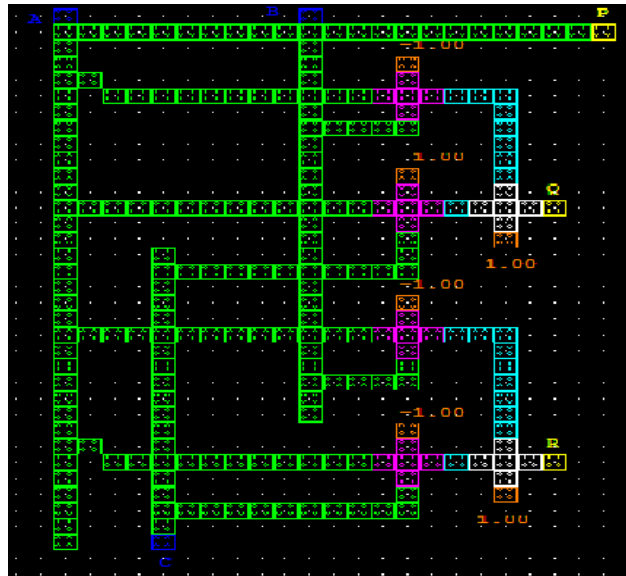


Fig.7. QCA layout for Fredkin gate

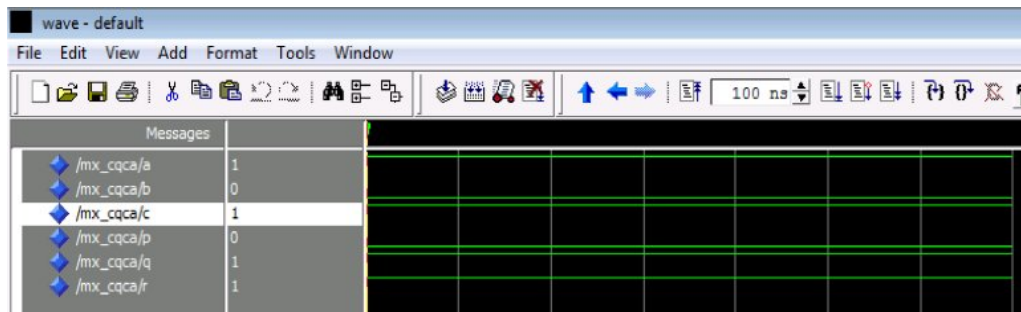


Fig. 8. HDL implementation of MX-CQCA (A=1, B=0, C=1 and I got the output P=0, Q=1, R=1)

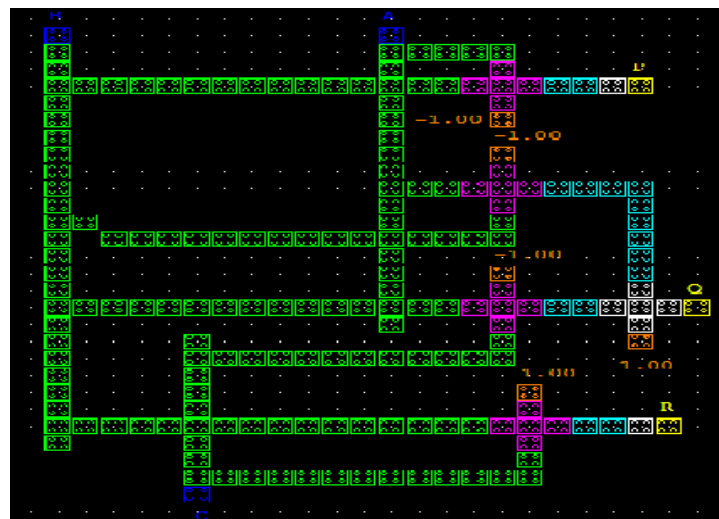


Fig. 9. QCA layout for MX-CQCA gate

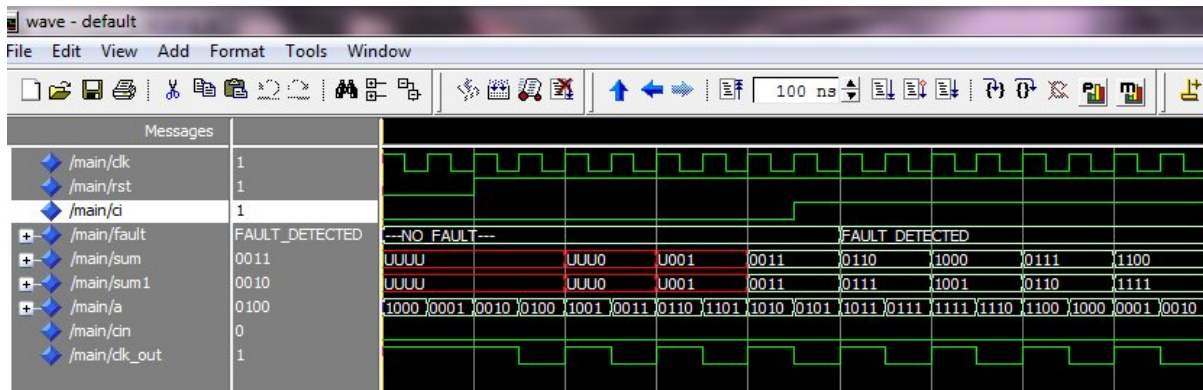


Fig.10. Simulation of full adder based ripple carry adder

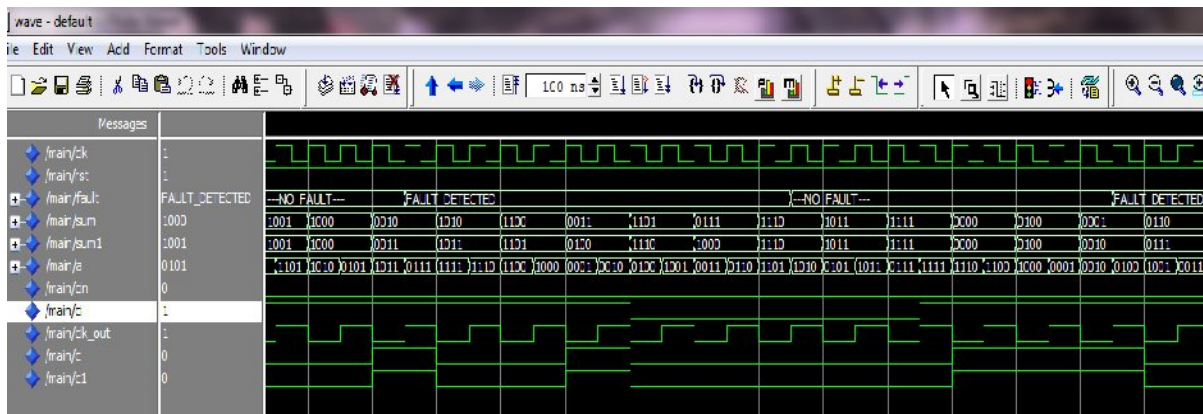


Fig.11. Simulation of MX-CQCA based ripple carry adder

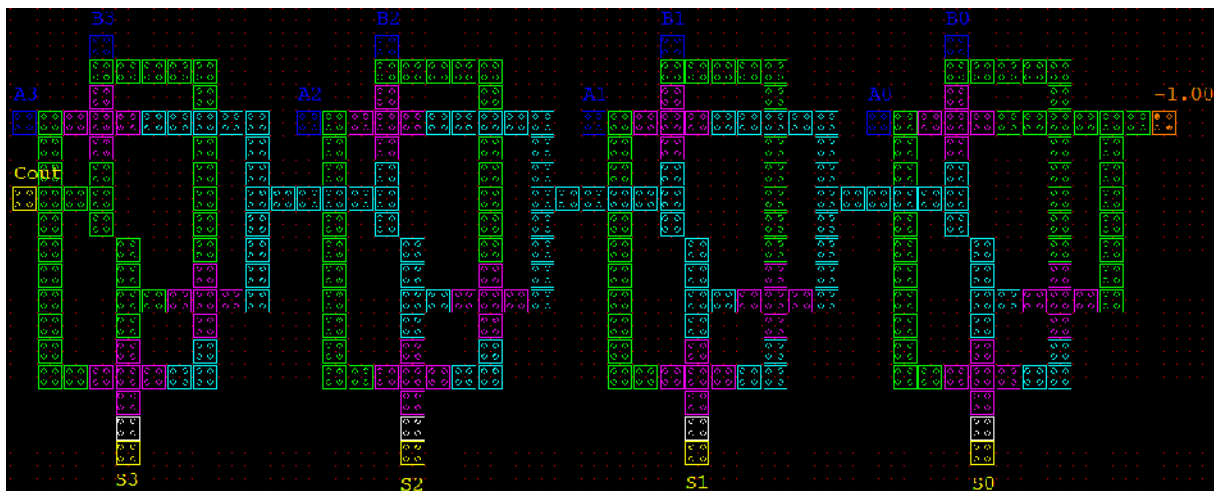


Fig.12. QCA layout for ripple carry adder using MX-CQCA

Table IV shows the comparison for Fredkin gate and MX-CQCA. This comparison is based on the QCA layout. MX-CQCA gate requires less number of majority voters than the Fredkin gate. The total number of QCA cells required is

are reduced by 22% compared to Fredkin gate and hence the power consumption of the MX-CQCA gate is less compared to Fredkin gate.





TABLE IV: COMPARISON OF FREDKIN GATE AND MX-CQCA GATE

| Parameter       | Fredkin gate | MX-CQCA gate |
|-----------------|--------------|--------------|
| Majority voters | 6            | 5            |
| Clock zones     | 4            | 4            |
| Total cells     | 231          | 190          |

TABLE V: COMPARISON OF FULL ADDER BASED RCA AND MX-CQCA BASED RCA

| Parameter | FA based RCA | MX-CQCA based RCA |
|-----------|--------------|-------------------|
| Area      | 220 gates    | 312 gates         |
| Delay     | 6.140ns      | 6.140ns           |
| Power     | 28mw         | 25mw              |

Figure 10 and Figure 11 show the HDL simulation of full adder based ripple carry adder and MX-CQCA based ripple carry adder respectively. Table 5 shows the comparison table for FA based RCA and MX-CQCA based RCA. The power, area and delay parameters are calculated by using Xilinx software and compared. The power consumption of the full adder circuit is reduced by using MX-CQCA. Figure 12 shows the QCA layout for ripple carry adder using MX-CQCA. In this layout, A0, A1, A2, A3, B0, B1, B2, B3 are the inputs and S0, S1, S2, S3 are the outputs.

## VI. CONCLUSION

This paper presented quantum dot cellular automata based full added design. This implementation used MX-CQCA to design a 4-bit ripple carry adder. The design process is carried out in Xilinx environment and the QCA layout of the 4-bit ripple carry adder is designed using QCADesigner software. Our experimental results show that the MX-CQCA based ripple carry adder consumes less power compared to Fredkin gate based ripple carry adder.

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