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Design and analysis of 63 to 6 compressor for the use of digital multipliers

G.M.G. Madhuri
Department of Electronics and Communication Engineering
PSCMR College of Engineering and Technology
Vijayawada, India
gmgmadhuri@gmail.com

G. Pavan Kumar
Department of Electronics and Communication Engineering
PSCMR College of Engineering and Technology
Vijayawada, India
pavankumargudisa@gmail.com

N. Cheatana Spoorthy Manogna
Department of Electronics and Communication Engineering
PSCMR College of Engineering and Technology
Vijayawada, India
nagubandi.spoorthy24@gmail.com

A. Sivananda Kashyap
Department of Electronics and Communication Engineering
PSCMR College of Engineering and Technology
Vijayawada, India
sivanandkashyap21@gmail.com

L. Sai Babu
Department of Electronics and Communication Engineering
PSCMR College of Engineering and Technology
Vijayawada, India
saibabu19122002@gmail.com

E. Pavan Teja
Department of Electronics and Communication Engineering
PSCMR College of Engineering and Technology
Vijayawada, India
tejaeemani2115@gmail.com

***Abstract*—This paper presents the design and analysis of 63 to 6 compressor using 31 to 5 compressor and 15 to 4 compressor as a basic module and it is a comprehensive exploration aimed at optimizing digital multiplication operations. The focus revolves around developing an efficient 63 to 6 compressor circuit, strategically tailored for integration into digital multipliers. The design phase involves meticulous component selection and architecture considerations, balancing precision and complexity. This project not only delves into the intricacies ofcircuit design but also underscores the practical implications of the 63 to 6 compressor within the context of digital multipliers. By fine-tuning parameters and optimizing performance, the project aims to enhance the efficiency of digital multiplication, paving the way for advancements in computational systems and contributing to the ongoing evolution of digital circuitry. This 63 to 6 compressor is designedusing two 31 to 5 compressors, full adders and parallel adder.**

Keywords*— *63 to 6 compressor, 31 to 5 compressor, 5 to 3 compressors, parallel adders, 15 to 4 compressors, Full Adders, Digital Multipliers, Efficiency.

I. INTRODUCTION

As we know, Digital multiplication is a basic computing operation that is widely used in a variety of applications, including arithmetic calculations and signal processing. Improving digital multiplication processes' speed and efficiency is essential to raising computing performance. Designing and integrating effective compressor circuits into digital multipliers is a crucial part of optimizing digital multiplication processes. It is suggested to use approximate compressors that are created by truncating the outputs of accurate compressors.

[1] but roughly speaking, compressors with just two outputs are utilized [2]. The study [3] suggests building an estimated 15 to 4 compressor with a 5 to 3 compressor as the foundational module.

By employing half-adders to create a smaller set of product terms, the method accomplishes lossy compression of the partial product rows. In [5], simple OR gates are used as rough counters. A new family of compressors is shown in Ref., in which there are no carry outputs and the compressors' outputs have the same weight as their inputs.

These 63 : 6 compressors only come in use when the multiplier size is 64 x 64 a32 × 32 and 16 × 16bit multipliers [7]-[8]. Better power and speed values are obtained with high order compressors [9]-[11]. Yet compared to low order compressors, it takes up more space.

In [12], an N-bit multiplier was constructed using two N/2 bit sub-multipliers. The most significant N/2 multiplier was then constructed using two more N/4 sub-multipliers, and the least significant N/2 multiplier was then applied using N/4 multiplier. A Wallace tree then gathers each incomplete product after that. Every recommended approach has pros and cons of its own.

The structure of the paper is as follows. The Literature survey has been covered in chapter II. Chapter III elaborates on the estimated 5 to 3 compressor designs. Chapter IV provides the detailed design of 15 to 4 compressor. Chapter V provides a detailed design and analysis of 31 to 5 compressor. Chapter VI details about design and analysis of 63 to 6 compressor. At last, the conclusion is given.

II. LITERATURE SURVEY

This chapter describes the earlier designed compressor models such as 4-2 compressor. A literature review for a compressor entail looking at previously conducted studies, academic papers, and pertinent books that cover a range of topics related to compressing algorithms. The purpose of this survey is to gather baseline data, identify knowledge gaps, and provide guidance for the creation and enhancement of 63-6 compressors.

C.–H. Chang,[14] J. Gu, and M. Zhang, Designed Ultra-low voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits.

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O. Akbari, M. Kamal, A. Afzali-Kusha, and M. Pedram,[15] Designed Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers.
S. Venkatachalam and S.-B. Ko,[16] Designed Power and Area Efficient Approximate Multipliers.

Marimuthu R, Elsie Rezinold [17] Developed a Multiplier design using approximate 15-4 compressor and analysis of the multiplier.
S. Venkatachalam and S.-B. Ko.[18] Designed a approximate multiplier by using efficient power and area.

[4] proposed a system, this paper presents an effective field programmable gate array (FPGA)-based hardware implementation of a parallel key searching system for the brute-force attack on RC4 encryption. The design employs several novel key scheduling techniques to minimize the total number of cycles for each key search and uses on-chip memories of the FPGA to maximize the number of key searching units per chip.

R. Marimuthu, M. Pradeepkumar, D. Bansal, S. Balamurugan, and P.S Mallick,[20] Designed a 15-4 compressor on communication and signal processing of high speed and low power.

K. Bhardwaj, P.S. Mane, and J. Henkel,[21] Developed a power and area efficient approximate Wallace tree multiplier for error resilient systems.

Haoran Pei, Xilin Yi, Hang Zhou, and Yajuan, He designed a approximate 4-2 compressors based on the compensation characteristic which is consuming ultra-low power.

III. Design and Synthesis of 5 to 3 Compressor

This section represents the design of 5 to 3 compressor which consists of five inputs which are I0, I1, I2, I3, I4 and three outputs that are O0, O1, O2. Output of the compressor relies on number of 1's at input. In this paper, this module is known as compressor because it reduces five bits into three bits. We consider this as a basic module for 15 to 4 compressor.

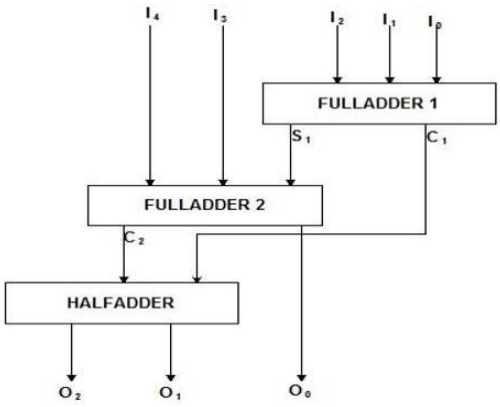

Fig 1: 5 to 3 compressor

IV. Design and Synthesis of 15 to 4 Compressor

This segment outlines the configuration of a 15 to 4 compressor employing 5 to 3 compressors. The 15 to 4 compressor, depicted in Fig.2, features fifteen inputs (X0 – X14) and yields four outputs (S0 – S3). The initial stage encompasses five full adders, followed by two 5 to 3 compressors in the second stage, and concludes with a modified parallel adder in the end stage. Each full adder takes three primary inputs, generating both sum and carry. [6] proposed a system, this paper presents an effective field programmable gate array (FPGA)-based hardware implementation of a parallel key searching system for the brute-force attack on RC4 encryption. The design employs several novel key scheduling techniques to minimize the total number of cycles for each key search and uses on-chip memories of the FPGA to maximize the number of key searching units per chip.. Compared to current designs, SEDAAF uses 25% less power and has a power delay product that is 17% lower.

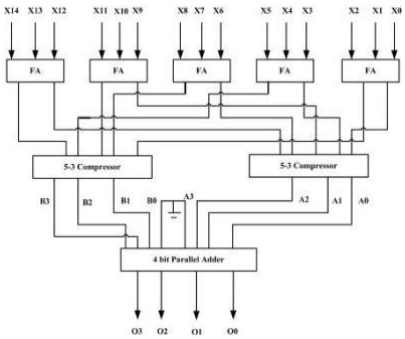

Fig 2: 15 to 4 compressor

V. Design and Synthesis of 31 to 5 Compressor

Here details of the design of 31 to 5 compressor circuit are explained. The 31 to 5 compressor has thirty-one primary inputs (X0, X1, X2, X3, X4…., X30) and five outputs (COUT, S3, S2,S1, S0). The compressor utilizes the counter property. The output of the compressor depends on the number of ones present at the input. In this paper, we label this submodule as acompressor because it compresses fifteen bits into four bits. We have selected the 15 to 4 compressor because it serves asa fundamental module for the 31 to 5 compressor. The block diagram is shown in Fig 3.

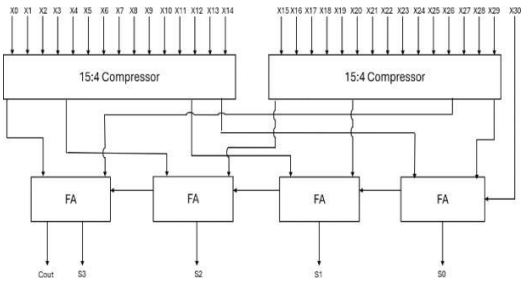

Fig 3: 31 to 5 compressor

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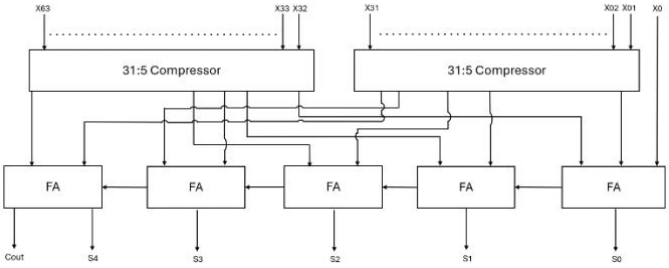
VI . DESIGN AND ANALYSIS OF 63 to 6 COMPRESSOR

This chapter explains the design and analysis of 63 to 6 compressor. As shown this module is of higher order in nature and has potential for being applied in key applications such as picture and audio signal refining while preserving essential information required for accurate multiplication. The compressor utilizes a combination of logic gates, carry chains, and parallel prefix adders to efficiently encode the input data into a compact representation. By eliminating redundant bits and exploiting data correlations, the compressor reduces the number of bits processed in subsequent addition stages, leading to improved overall performance.



VII. RESULTS

This chapter discusses the outcomes of the compressors after simulation. Fig 4a shows the schematic of 5 to 3 compressor and fig 4b shows the output waveform of 5 to 3 compressor. In fig 5a,5b the output waveform of 15 to 4 and schematic of 15 to 4 compressor respectively.

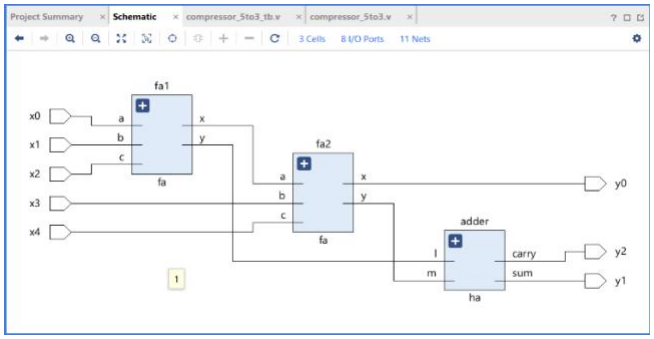


Fig 4a: Schematic of a 5 to 3 compressor

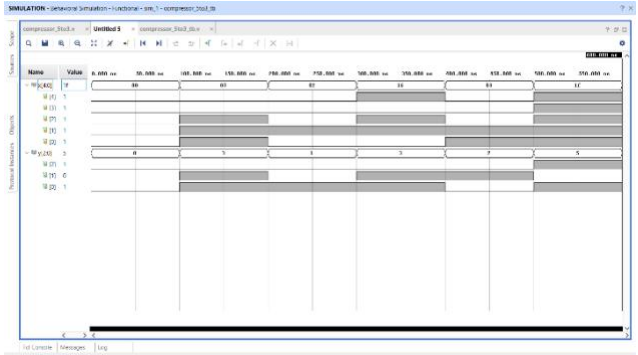


Fig 4b: Waveform of a 5 to 3 compressor

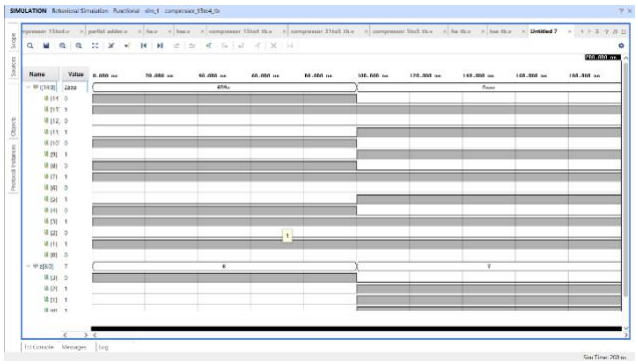


Fig 5a: Waveform of a 15 to 4 compressor

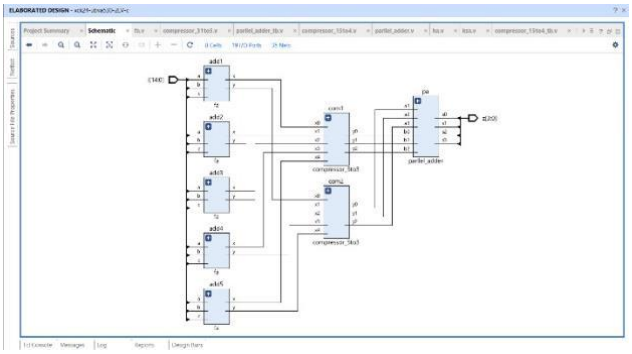


Fig 5b: Schematic of 15 to 4 compressor

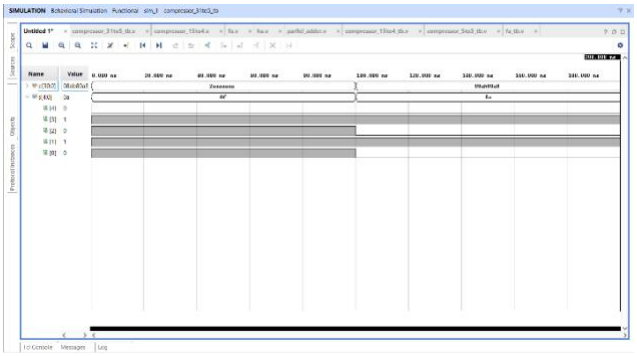


Fig 6a: Waveform of a 31 to 5 compressor

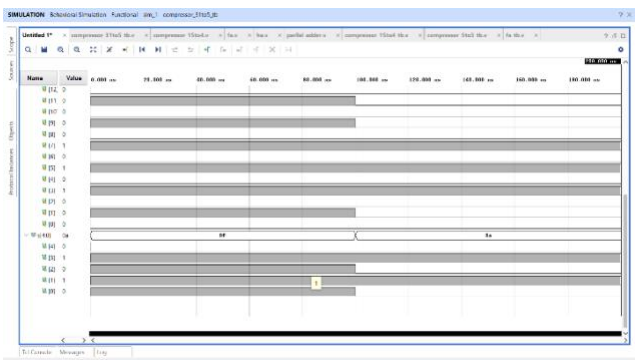


Fig 6b: Waveform of a 31 to 5 compressor

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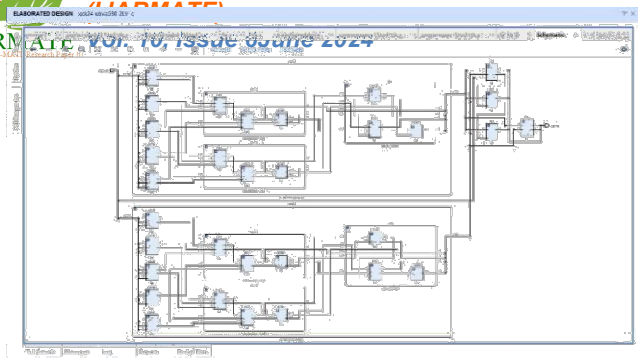
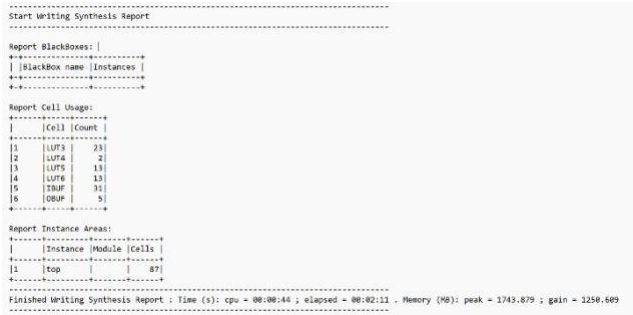


Fig 7: Schematic of a 31 to 5 compressor



```
Start Writing Synthesis Report

Report BlackBoxes:
+----+--------------+-----------+
|    |BlackBox name |Instances  |
+----+--------------+-----------+
+----+--------------+-----------+

Report Cell Usage:
+------+------+-------+
|      |Cell  |Count  |
+------+------+-------+
|1     |LUT3  |    23|
|2     |LUT4  |     2|
|3     |LUT5  |    13|
|4     |LUT6  |    13|
|5     |IBUF  |    31|
|6     |OBUF  |     5|
+------+------+-------+

Report Instance Areas:
+------+----------+------+-------+
|      |Instance  |Module|Cells  |
+------+----------+------+-------+
|1     |top       |      |    87|
+------+----------+------+-------+

Finished Writing Synthesis Report : Time (s): cpu = 00:00:44 ; elapsed = 00:02:11 . Memory (MB): peak = 1743.879 ; gain = 1250.609
```

Fig 8: Synthesis report of 31 to 5 compressor

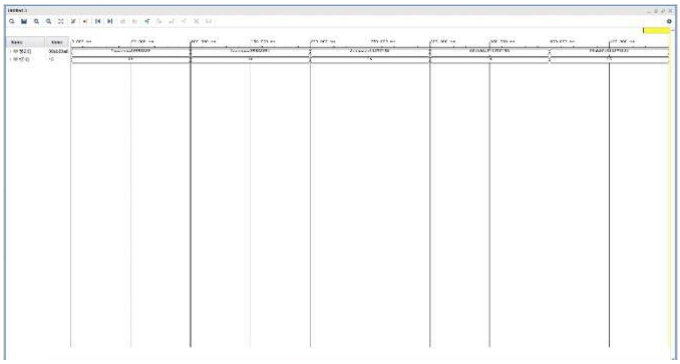


Fig 9: Waveform of a 63 to 6 compressor

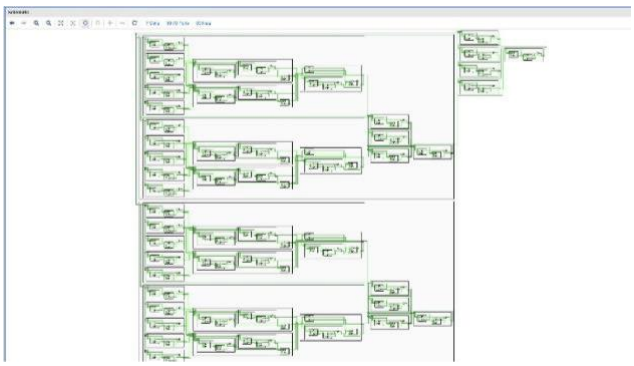


Fig 10 Schematic of 63 to 6 compressor

VIII. CONCLUSION

In conclusion, the design and analysis of the 63 to 6 compressor have yielded comprehensive insights into its performance characteristics across multiple domains, including power consumption, time efficiency, and energy utilization. Regarding power consumption, the compressor demonstrates an optimized design that ensures efficient utilization of resources. In terms of time efficiency, the compressor exhibits rapid processing capabilities without compromising compression quality. Concerning energy utilization, the compressor's design emphasizes sustainability and resource conservation.

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Bibliography

Dr. G. M. G Madhuri currently working as a professor in the department of Electronics and Communication Engineering, PSCMR College of Engineering and Technology, Vijayawada, Andhra Pradesh, India. She graduated with a bachelor's degree in Electronics & Communication Engineering from JNTUH Andhra Pradesh, master's degree in VLSI System Design from Nimra Institute of engineering and technology JNTUK, Andhra Pradesh. She is a member of IAENG, ISSE and IEEE.

Mr. G. Pavan Kumar currently pursing final year in the department of Electronics and Communication Engineering, PSCMR College of engineering and Technology, Vijayawada, Andhra Pradesh, India. He is a member of IETE. Since his keen interest in VLSI, Design and verification.

Ms. N. Chetana Spoorthy Manogna currently pursing final year in the department of Electronics and Communication Engineering, PSCMR College of engineering and Technology, Vijayawada, Andhra Pradesh, India. She is a member of IETE. Since her keen interest in VLSI, Design and verification.

Mr. A. Sivananda Kashyap currently pursuing final year in the department of Electronics and Communication engineering, PSCMR College of Engineering and Technology, Vijayawada, Andhra Pradesh, India. He is a member of IETE. His interest in VLSI, Design and Verification.

Mr. L. Sai Babu currently pursing final year in the department of Electronics and Communication Engineering, PSCMR College of Engineering and Technology, Vijayawada, Andhra Pradesh, India. He is a member of IETE. Since his keen interest in VLSI, Design and verification

Mr. E. Pavan Teja currently pursuing final year in the department of Electronics and Communication Engineering, PSCMR College of Engineering and Technology, Vijayawada, Andhra Pradesh, India. He is a member of IETE. His interest in VLSI, Design and Verification.