Design of Area Efficient Parallel Filter for Tolerating Error

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***Abstract* -- Digital filters are mainly used in signal processing and communication systems where reliability is critical. To overcome this reliability problem fault tolerant filter implementations is used. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, a weight padding technique is proposed to achieve fault tolerance in the parallel filter. This approach uses each of the filter outputs as the equivalent of a bit in and ECC codeword. This method uses only two redundant filters i.e. all the inputs are added with different weights, so that if error occurs the redundant module recovers the faulted input to produce the exact output without affecting the system functionality. It recovers the output compare to existing. This scheme can also be used to provide more powerful protection using advanced ECCs that can correct failures in multiple modules.**

***Index Terms*- Error correction code (ECCs), filters.**

I. INTRODUCTION

Electronic circuits are increasingly present in automotive, medical and space applications where reliability is critical. In those applications, the circuits have to provide some degree of fault tolerance. This need is further increased by the intrinsic reliability challenges of advanced CMOS technologies that include, e.g., manufacturing variations and soft errors. In electronics and computing, a soft error is a type of error where a signal or datum is wrong. Errors may be caused by a defect, usually understood either to be a mistake in design or construction, or a broken component. After observing a soft error, there is no implication that the system is any less reliable than before. In the spacecraft industry this kind of error is called a single-event upset.

A number of techniques can be used to protect a circuit from errors. One commonly used technique is modular redundancy whereby the circuit to be protected is replicated *N* times and extra logic is added to detect and correct errors. In the case that *N* equals two, the technique is known as dual modular redundancy (DMR). In DMR, the outputs of two identical modules are compared, and an error is detected if the outputs differ. Conventional DMR does not provide error correction. In the case that *N* equals three, the technique is known as triple modular redundancy (TMR). The TMR, which triplicates the design and adds voting logic to correct errors, is commonly used. However, it more than triples the area and power of the circuit, something that may not be acceptable in many applications.

Hamming code is a set of error-correction codes that can be used to detect and correct bit errors. Like other error-correction code, Hamming code makes use of the concept of parity and parity bits, which are bits that are added to data so that the validity of the data can be checked when it is read or after it has been received in a data transmission. Using more than one parity bit, an error-correction code can not only identify a single bit error in the data unit, but also its location in the data unit. If the number of parallel filters in the original module is increased then the number of parallel filters in the redundant module is also increased.

In this brief, a weight padding technique to protect parallel filters is presented. This approach uses each of the filter outputs as the equivalent of a bit in and ECC codeword. Proposed method uses only two redundant filters i.e. all the inputs are added with different weights, so that if error occurs the redundant module recovers the faulted input to produce the exact output without affecting the system functionality. This is a generalization of the scheme presented in and enables more efficient implementations when the number of parallel filters is large. The scheme can also be used to provide more powerful protection using advanced ECCs that can correct failures in multiples modules.

II. PARALLEL FILTER WITH THE SAME RESPONSE

A discrete time filter implements the following equation:

$$y[n] = \sum_{l=0}^{\infty} x[n-l].h[l] \qquad (1)$$

Where x[n] is the input signal, y[n] is the output, and h[l]is the impulse response of the filter. When the response h[l] is nonzero, only for a finite number of samples, the filter is known as a FIR filter, otherwise the filter is an infinite impulse response (IIR) filter. There are several structures to implement both FIR and IIR filters.

In the following, a set of k parallel filters with the same response and different input signals are considered. These parallel filters are illustrated in Fig. 1. This kind of filter is found in some communication systems that use several channels in parallel. In data acquisition and processing applications is also common to filter several signals with the same response.

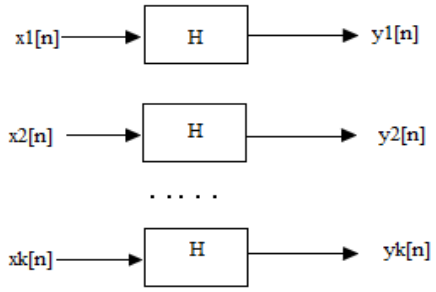


Fig. 1. Parallel filters with the same response.

III. PROPOSED SCHEME

This approach uses each of the filter outputs as the equivalent of a bit in and ECC codeword. Proposed method uses only two redundant filters i.e. all the inputs are added with different weights, so that if error occurs the redundant module recovers the faulted input to produce the exact output without affecting the system functionality. It recovers the output compare to existing. For example a system consists of four different inputs. Each is given by different input. In ECC it takes copy for the each input. When an error occurs, the system uses redundant modules to recover the corrupted input to get output. The module that is uses a copy called redundant module.

This weight padding technique can also be used to provide more powerful protection using advanced ECCs that can correct failures in multiple modules. For example the original module having four or many input results correct output. Each output has a combination of corresponding input in temporary error correcting coding module. If there is error in any one of the input the temporary ECC consisting three modules is taken, of these the module having the combination of the defected input is detected and finally corrected. It is used correct multiple errors.

Here the input x5 and x6 are obtained as follows

$$X5=w11.x1+ w12.x2+ w13.x3+ w14.x4$$

$$X6=w21.x1+ w22.x2+ w23.x3+ w24.x4 \quad (3)$$

Where w11 to w14 and w21 to w24 are different weights used to differentiate the inputs, so that it will be easy to identify whether or not an error has occurred and it will be easy to correct it. This new scheme provides more efficient protection when the number of parallel filters is large, since redundant filters are independent of the number of parallel filters.

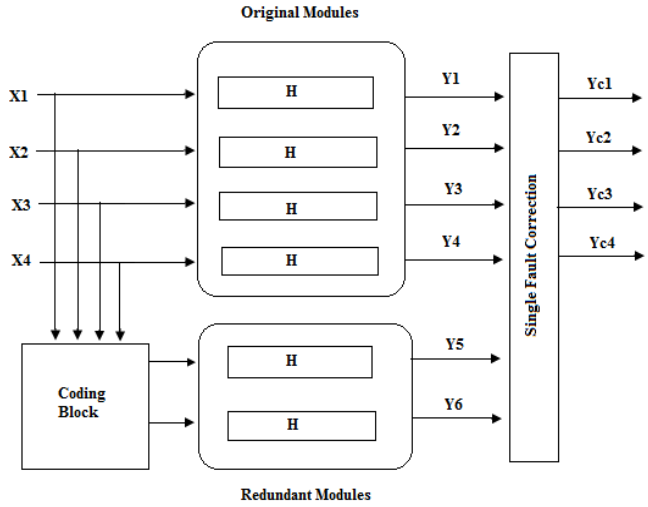


Fig. 2. Block diagram for proposed scheme

Here the redundant module inputs X5 and X6 are obtained as follows:

$$X5= X1+X2+X3+X4$$

$$X6= X1+2.X2+3.X3+4.X4 \quad (4)$$

The error detection is done by testing if

$$P1=P2=0 \text{ (no error)}$$

$$P1 \neq 0; P2 \neq 0 \text{ (error)} \quad (5)$$

Where P1 and P2 are computed as

$$Y5–[Y1+Y2+Y3+Y4] =P_1$$

$$Y6–[Y1+2.Y2+3.Y3+4.Y4] =P_2 \quad (6)$$

TABLE I

ERROR LOCATION IN WEIGHT PADDING TECHNIGUE

Conditions	Error bit position	Action
P1=P2=0	No error	None
P1 ≠0; P2 ≠0	Error	Correction need
P1=P2≠0	Y1	Corrected Y1
2.P1=P2	Y2	Corrected Y2
3.P1=P2	Y3	Corrected Y3
4.P1=P2	Y4	Corrected Y4

For the filter, correction is achieved by

$$YC1= Y5 – [Y2+Y3+Y4]$$

YC2= Y5 – [Y1+Y3+Y4]

YC3= Y5 – [Y1+Y2+Y4]

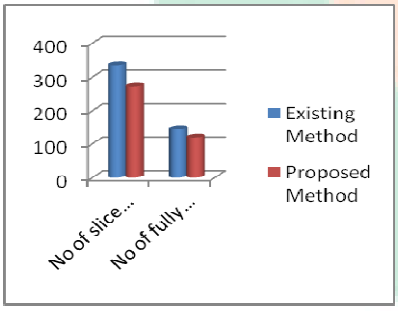
YC4= Y5 – [Y1+Y2+Y3] (7)

TABLE II

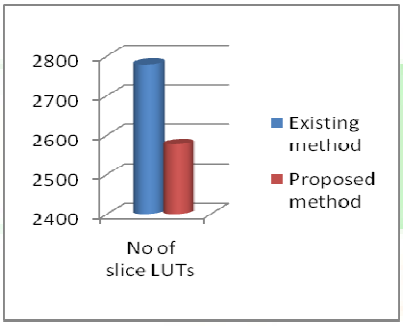
RESOURCE COMPARISON FOR FOUR PARALLEL FILTERS

PARAMETER	EXISTING METHOD	PROPOSED METHOD
No of slice registers	336	271
No of slice LUTs	2780	2576
No of fully used LUT-FF pairs	145	119
No of DSP-48A1s	25	22
Total CPU time	49.33 sec	39.07 sec

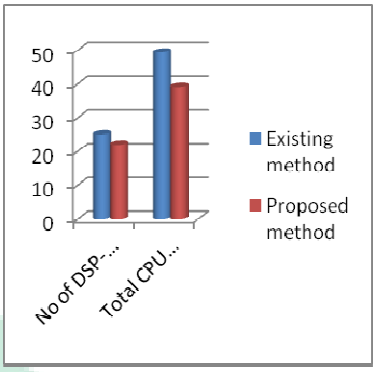
From the above tabulation it is clear that the proposed method requires only less time to complete the process compared to the existing method.



(a)



(b)



(c)

Fig. 3. Comparison among the weight padding system. (a) Comparison of LUT-FF pair. (b)Comparison of Slice. (c)Comparison of DSP.

In Fig. 3 (a), (b) and (c), we have introduced the plot for the proposed work slice LUTs, LUT-FF and DSP-48A 1s using weight padding method. In these graph our proposed work outperforms well than the existing method the total CPU time is lower for the proposed work which gives 39.07 sec.

IV. CONCLUSION

A new scheme to protect parallel filters that are commonly found in modern signal processing circuits. The approach is based on applying ECCs to the parallel filters outputs to detect and correct errors. The scheme can be used for parallel filters that have the same response and process different input signals. This technique provides larger benefits compare to others. The proposed scheme can also be applied to the IIR filters.

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