Design Of An Efficient Encoder For DSRC Application Using SOLS Technique

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Abstract: Dedicated short-range communication (DSRC) plays an important role in intelligent transportation system applications. DSRC standards usually adopt FM0 code and Manchester code as a coding technique to enhance signal reliability, but the diversity in coding technique limits the possibility for designing a reused VLSI architecture for both the encoding methods. In this paper propose a technique called similarity-oriented logic simplification (SOLS) technique to overcome the limitation. This SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. To achieve fully reused VLSI architecture of FM0/Manchester codec with maximum hardware utilization rate (HUR) half-cycle processing model can be used.

I. INTRODUCTION

The dedicated short-range communication (DSRC) is a protocol for one- or two-way medium range communication especially for intelligent transportation systems. Using a modified IEEE 802.11a technology for North American cars and trucks, DSRC is designed for several applications. For example, ambulances can cause traffic lights down the road to change in their favor, and traffic congestion can be transmitted to automobile navigation systems. It allows vehicles to sense that they are about to crash, and the safety systems can begin to tighten seatbelts and warm up the airbags before impact. In addition, a standard for wireless payment allows parking lots and fast-food drive-ins to offer the same convenience as the automated highway toll systems such as E-ZPass.

The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC enables the message-sending and broadcasting among automobiles for safety issues and public information announcement. The safety issues include blind-spot, intersection warning, inter cars distance, and collision-alarm. The automobile-to-roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC) system. With ETC, the toll-collecting is electrically accomplished with the contactless IC-card platform. Moreover, the ETC can be extended to the payment for parking-service, and gas-refueling. Thus, the DSRC system plays an important role in modern automobile industry.

The system architecture of DSRC transceiver is shown in Fig. 1. The upper and bottom parts are dedicated for transmission and receiving, respectively. This transceiver is classified into three basic modules

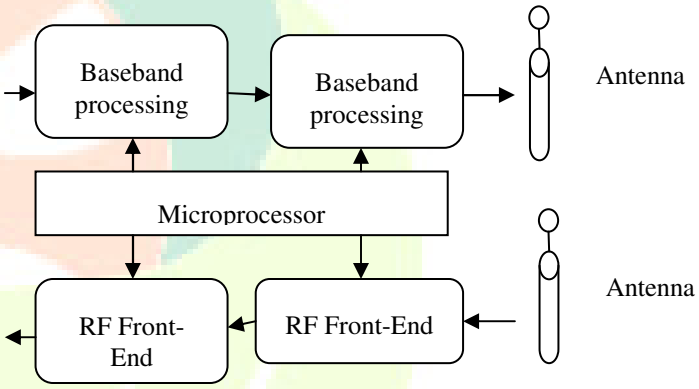


Fig 1 block diagram

- Microprocessor
  - The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end.
- Baseband processing
  - The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding.
- RF front-end
  - The RF front-end transmits and receives the wireless signal through the antenna.

Manchester encoding is also called phase encoding. It can be used for a higher operating frequency. Manchester encoding is a very common method and is probably the most commonly used. The signals can be transmitted serially. In Manchester encoding the average power is always the same, no matter what data is transmitted. Compared to all other encoding methods, Manchester code follows an algorithm to encode the data. It always produces a transition at the center of the bit. It contains sufficient information to recover a clock. So if the data rate is twice, sufficient clock information can be

recovered from the data stream so that separate clocks are not needed.

II. LITERATURE REVIEW

J. B. Kenney proposed "Dedicated Short-Range Communications (DSRC) Standards in the United States"[2]. Wireless vehicular communication has the potential to enable a host of new applications, the most important of which are a class of safety applications that can prevent collisions and save thousands of lives. The automotive industry is working to develop the dedicated short-range communication (DSRC) technology, for use in vehicle-to-vehicle and vehicle-to-roadside communication. The effectiveness of this technology is highly dependent on cooperative standards for interoperability. Included in the discussion are the IEEE 802.11p amendment for wireless access in vehicular environments (WAVE), the IEEE 1609.2, 1609.3, and 1609.4 standards for Security, Network Services and Multi-Channel Operation, the SAE J2735 Message Set Dictionary, and the emerging SAE J2945.1 Communication Minimum Performance Requirements standard. The paper shows how these standards fit together to provide a comprehensive solution for DSRC The coding-diversity between the two codes seriously limits the potential to design a fully reused VLSI architecture

V. Taliwal and A. Meier proposed "Design of 5.9 GHz DSRC-based vehicular safety communication"[3]. The automotive industry is moving aggressively in the direction of advanced active safety. Dedicated short-range communication (DSRC) is a key enabling technology for the next generation of communication-based safety applications. One aspect of vehicular safety communication is the routine broadcast of messages among all equipped vehicles. Therefore, channel congestion control and broadcast performance improvement are of particular concern and need to be addressed in the overall protocol design. Furthermore, the explicit multichannel nature of DSRC necessitates a concurrent multichannel operational scheme for safety and non-safety applications. This article provides an overview of DSRC based vehicular safety communications and proposes a coherent set of protocols to address these requirementsThe SOI process not suitable for power devices

M. A. Khan and M. Sharma proposed "FSM based FM0 and Miller encoder for UHF RFID tag emulator"[7]. The radio frequency identification system (RFID) is becoming very popular system wireless technologies. The UHF RFID tag emulator is a part of RFID testing tools. The UHF RFID tag emulator would be imitating the behavior of RFID Tag. The UHF RFID tag emulator (860 Mhz to 960 MHz) is aimed for testing the RFID systems and also as a general-purpose communication link to other electronic devices. In this work, we have presented high-level architecture of tag emulator and the design of FM0 encoder and Miller encoder. As motivated by finite state machine, encoders are discussed with particular focus to use the RFID emulator as data transport device and debugging tool. The synthesis result shows that FSM design is efficient and we have achieved operating frequency of 192.641 MHz and 188.644 MHz for FM0 and Miller encoders. It can generate electromagnetic interference (EMI) effect to jam other circuits External wireless signals to endanger the reliability. Lot of discrete components, i.e., transformer and capacitor.

H. Zhou and A. Aziz proposed "Buffer minimization in pass transistor logic"[11]. With shrinking feature sizes and increasing transistor counts on chips, demands for higher speed and lower power make it necessary to look for alternative design styles that offer better performance than static complementary metal-oxide-semiconductors. Among them, pass transistor logic (PTL) is of great promise. Since delay in a transistor chain is quadratically proportional to the number of transistors and a signal may degenerate passing through a transistor, buffers are necessary to guarantee performance and restore signal strength in PTL circuits. In this paper, we first analyze effects of buffer insertion on a circuit and give a sufficient and necessary condition for safe buffer insertion. Then, a buffer minimization problem is formulated. Although it is NP-hard in general, it can be solved linearly when buffers are required on multi fan-out nodes. We also consider the case when buffers are inverters, where phase assignment needs to be done with buffer insertion Many external components are used

M.-M. Kuo and C.-K. Tung proposed "High-speed CMOS chip design for Manchester and Miller encode"[6]. In this paper, a modified Manchester and Miller encoder that can operate in high frequency without a sophisticated circuit structure is proposed. Based on the previous proposed architecture, the study has adopted the concept of parallel operation to improve data throughput. In addition, the technique of hardware sharing is adopted in this design to reduce the number of transistors. External wireless signals to endanger the reliability.

III EXISTING SYSTEM

Fm0 encoding :

Transition occurs at the beginning of each clock cycle.

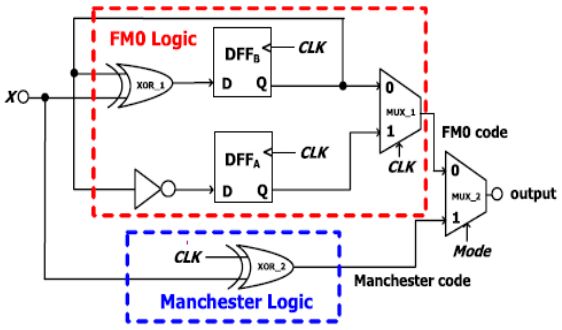
Binary 0 → additional transition at the middle of clock cycle

Binary 1 → no transition at the middle of clock cycle

3.1Area-Compact Retiming

The FM0 logic shows the logic for A(t) and the logic for B(t) are the Boolean functions to derive A(t) and B(t),where the X is omitted for a concise representation. For

FM0, the state code of each state is stored into DFFA and DFFB.



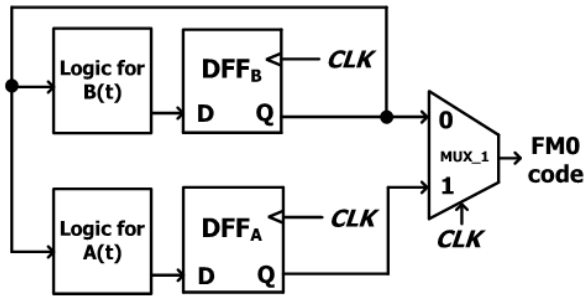


Fig 3.1 FM0 encoding

Thus, the FM0 encoding just requires a single 1-bit flip-flop to store the B(t−1).If the DFFA is directly removed, a non synchronization between A(t) and B(t) causes the logic-fault of FM0 code. To avoid this logic-fault, the DFFB is relocated right after the MUX−1, as shown in Fig. 4, where the DFFB is assumed to be positive-edge triggered. At each cycle, the FM0 code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FM0 code is alternatively switched between A(t) and B(t) through the MUX−1 by the control signal of the CLK.

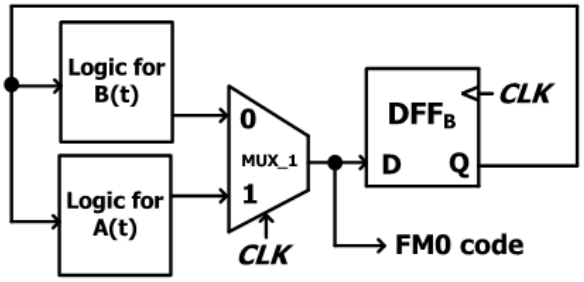


Fig 3.2 FM0 encoding with area-compact retiming

Above Fig shows the Q of DFFB is directly updated from the logic of B(t) with 1-cycle latency. when the CLK is logic-0, the B(t) is passed through MUX−1tothe D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB.

3.2 Balance Logic-Operation Sharing

The Manchester encoding can be derived from X ⊕ CLK, and it is also equivalent to

$$X \oplus CLK = X\,CLK + X\,CLK.$$

This can be realized by the multiplexer, as shown in Fig.5(a). It is quite similar to the Boolean function of FM0 encoding. The FM0 and Manchester logics have a common point of the multiplexer-like logic with the selection of CLK. As shown in Fig. 5(b), the concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t), respectively. The logic for A(t)/X is shown in Fig.5(c).The A(t) can be derived from an inverter of B(t − 1),and X is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch the operands of B(t − 1) and X. The Mode indicates either FM0 or Manchester encoding is adopted

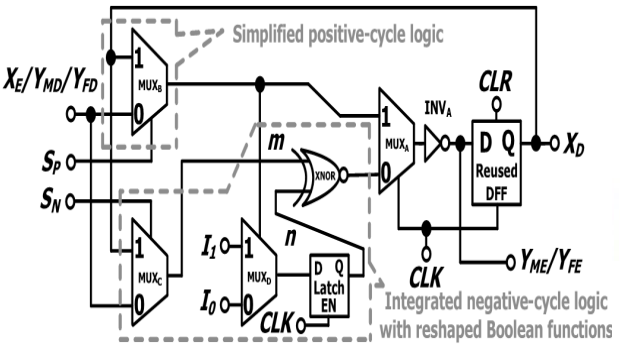
IV PROPOSED SYSTEM

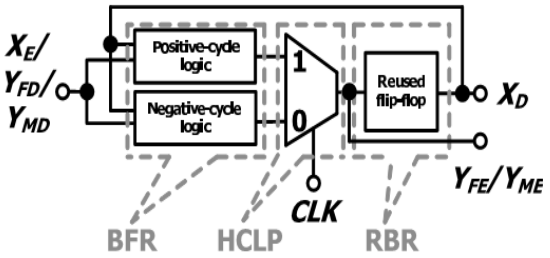
The proposed FM0/Manchester codec supports fourcoding modes, including FM0 encoding/decoding and Manchester encoding/decoding.

The HCPM includes three core techniques:

[1] Half-cycle logic partition;
[2] Reused-based retiming; and
[3] Boolean function reshaping.

The proposed VLSI architecture of FM0/Manchester codec is based on HCPM. The HCPM is a model of the hardware architecture for FM0/Manchester codec. It classifies FM0/Manchester encoding and decoding into two parts: positive-cycle signal and negative-cycle signal. Both are manipulated by positive-cycle logic and negative-cycle logic, respectively. With this classification, the function of FM0/Manchester codec can be transformed into the HCPM as illustrated in Fig below. The HCPM model consists of three core techniques: HCLP, RBR, and BFR.



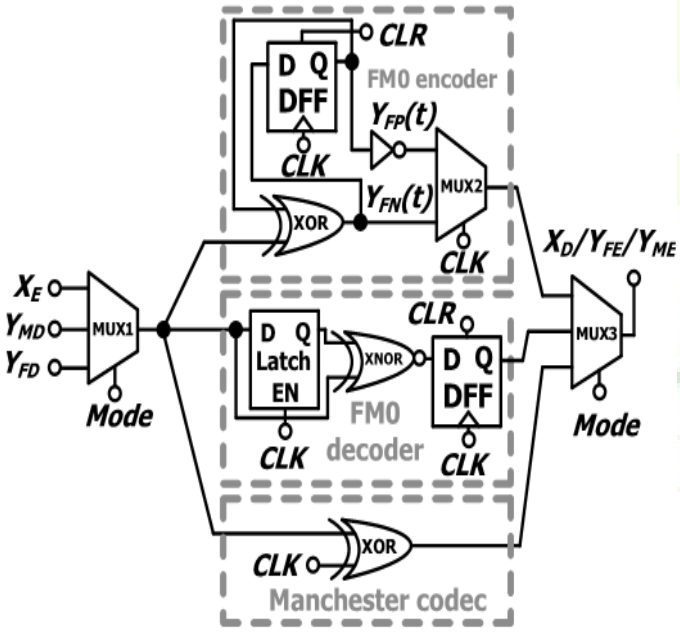


The HCLP classifies FM0/Manchester encoding and decoding into the positive-cycle logic and the negative-cycle logic. Then, a 2-to-1 multiplexer is allocated after them to sequentially present positive-cycle signal and negative-cycle signal by CLK. The RBR can conduct a reused flip-flop from the positive-cycle logic and the negative-cycle logic. This reused flip-flop is located after the 2-to-1 multiplexer to separate the output data paths of FM0/Manchester encoding and decoding. If FM0/Manchester encoding is adopted, the output of the 2-to-1 multiplexer presents YME /YFE. If FM0/Manchester decoding is adopted, the XD is presented on the output of the reused flip-flop. With HCLP and RBR, the BFR further simplifies positive-cycle logic and integrates negative-cycle logic.

HCLP

The FM0 encoding is naturally conducted from positive-cycle logic YFP(t) and negative-cycle logic YFN (t).Discussionmainlyfocuses on the positive-cycle logic and the negative-cyclelogic of Manchester encoding/decoding and FM0 decoding.

RBR Technique



As earlier shown in the above Fig, only FM0 encoder andFM0 decoder require a DFF.The HUR ofFM0/Manchester codec can be greatly improved, if the DFFcan be reused. It is the purpose of RBR to conduct a reusedDFF from positive-cycle logic and negative-cycle logic inFM0/Manchester encoding and decoding.

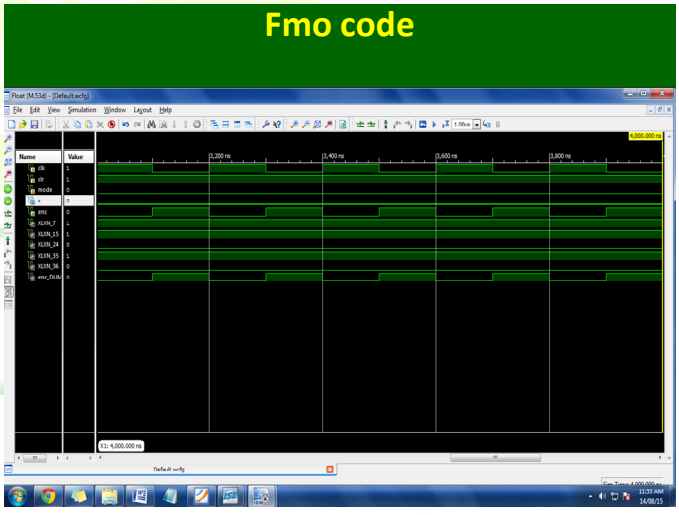
BFR Technique

The purpose of BFR is to simplify positive-cycle logic andintegrate negative-cycle logic. The simplified positive-cyclelogic and the integrated negative-cycle logic are individuallydiscussed in following subsections.

- Simplified Positive-Cycle Logic
- Integrated Negative-Cycle Logic

V CONCLUSION AND FINAL RESULTS

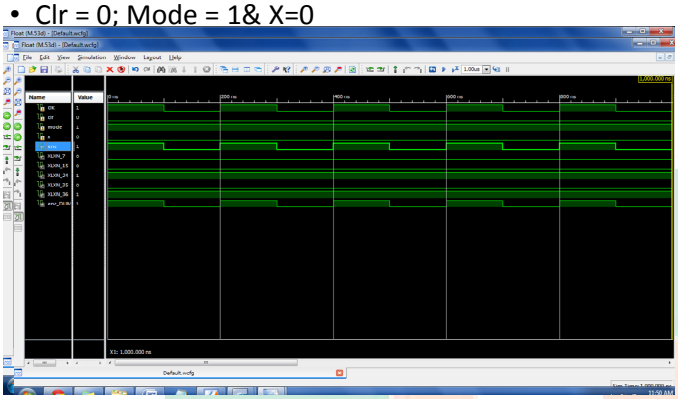
The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSIarchitecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed indetail. In this paper, the fully reused VLSI architecture usingSOLS technique for both FM0 and Manchester encodingsis proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area-compact retiming and balance logic-operation sharing. Thearea-compact retiming relocates the hardware resource toreduce the number of transistors. The balance logic-operation sharingefficiently combines FM0 and Manchester encodings with theidentical logic components. The encodingcapability of this paper can fully support the DSRC standardsof America, Europe, and Japan. This paper not only develops afully reused VLSI architecture, but also exhibits a competitiveperformance compared with the existing works

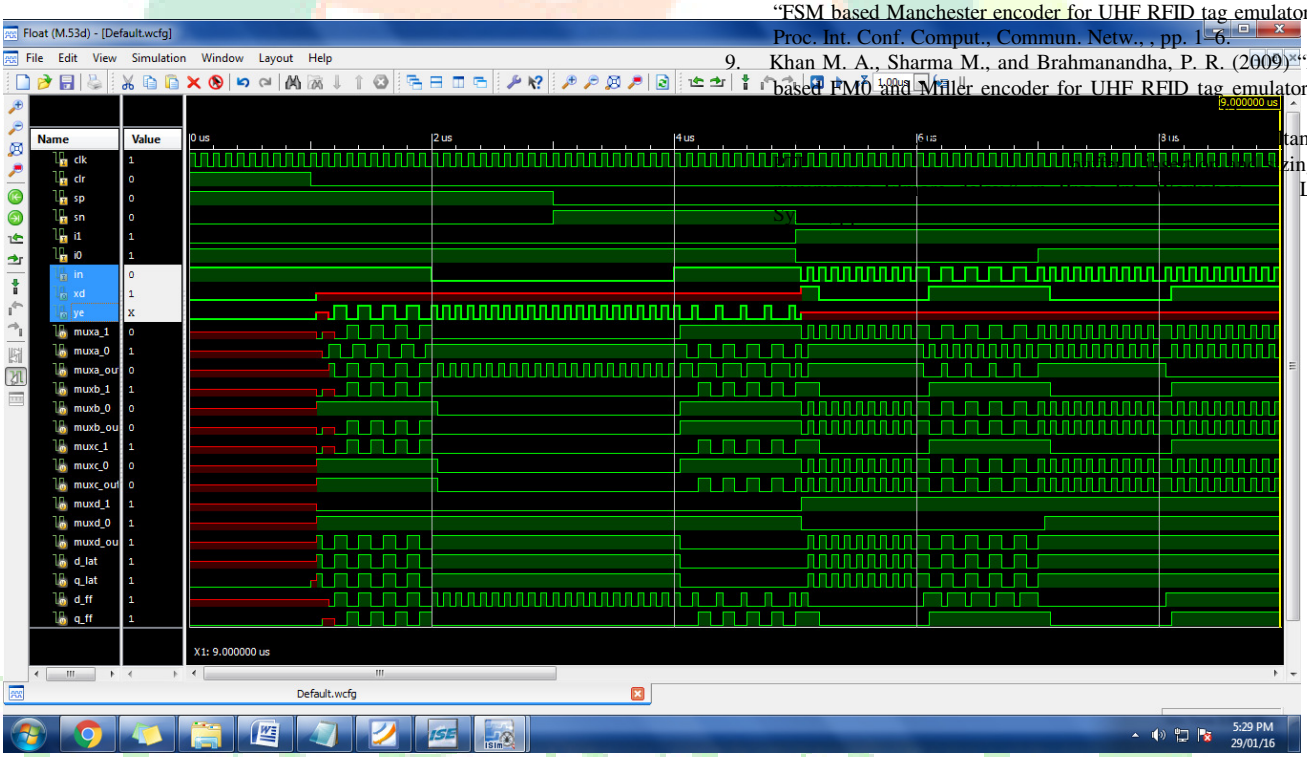


In this paper ,decoder circuit to be used to achieve hardware utilization rate and to improve the dc balancing.

Screenshot for Manchester codes
Clr = 0; Mode = 1& X=0

- Clr = 0; Mode = 1& X=0





Coding mode	S_P	S_N	I_1	I_0
FM0 encoding	1	0	0	1
FM0 decoding	0	0	1	0
Manchester encoding	0	1	0	1
Manchester decoding	0	0	1	1

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