Design of DRAM using Low Power DLL with TDC

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***Abstract*— This project proposes a 90° phase-shift delay-locked loop (DLL) used in dynamic RAM for data sampling clock generation and clock synchronization. In previous DLL, the mismatch between the delay line segments which caused the process variation in the circuit. This proposed DLL reduce the process variation issues and also minimize the area by adopting a multiplying DLL based structure. The harmonic locking problem is prevented by a ring oscillator. The fine delay range selector and the resistance controlled fine delay unit is used to achieve a fast operating frequency with a finer resolution. The proposed system is verified through design in a standard 250nm CMOS process supplied by Tanner's EDA simulation software tool and it utilizes 1.8V supply voltage. The proposed DLL has an operating frequency ranging from 250MHz to 5GHz and consumes 10.2mW at 5GHz .The entire proposed All digital 90° phase-shift delay-locked loop (DLL) is designed and the layout of this system through Tanner EDA Software is implemented.**

Keywords—90° phase-shift; delay-locked loop (DLL); CMOS; Tanner EDA

I.INTRODUCTION

Delay-Locked Loops (DLLs) are widely used in memory applications to perform tasks such as clock synchronization and strobe signal generation [1]–[6]; for instance, a 90° phase-shift DLL is used to shift the data strobe signal by 90° for data sampling [7]–[9]. As the data-rate requirements of dynamic RAM (DRAM) increase, the timing margin for data sampling in the DRAM I/O becomes worse; correspondingly, highly accurate 90° phase shifting and low-jitter performance are significant DLL design factors.

To process this larger quantity of multimedia data, there is a demand for improved system performance. To satisfy this requirement, the operating frequency has been increased and more transistors have been integrated into a chip by technology scaling. However, this has brought side effects such as a decrease in the timing margin because of the shorter clock period, an increase in process variation caused by the smaller transistor size, and larger power consumption as the result of the high operating frequency and large number of integrated transistors. We also need lot of capacitor and charge pump or additional output buffer to control the delay of each delay units.

The timing margin of the memory system is also affected by clock jitter, which is responsible for two significant timing issues: 1) jitter peaking and 2) dithering jitter. Jitter peaking is a phenomenon in which noise within a certain frequency range is amplified in the output clock ,whereas dithering jitter is caused by dithering of the control code of a delay line, especially in digital DLLs.

In previous DLLs, the analog DLL in [2]–[3] also have power and area hungry components such as a charge pump and capacitor. Moreover, they cannot operate at a low supply voltage because the analog component must operate in the active region. To minimize the analog circuitry, the digital DLL whose loop filter is implemented by the digital circuit is adopted but DDLL also requires analog circuitry such as digital- to-analog converter (DAC) for VCDL[4]. Recently, the all-digital 90 phase shift DLL whose 90 phase shift delay line consists of a coarse delay line (CDL) and a fine delay line (FDL) has been adopted to overcome these weaknesses of the analog and digital DLLs [5],[6]. The problem with this structure is the mismatch among the delay-line segments owing to process variation [1]–[3], which will affect the accuracy of the 90° phase shift and worsen the timing margin. To solve this problem, proposed dithering suppression loop controller (DSLC) will become vulnerable to external noise or variations and also suppress the code dithering.

In this paper, All digital 90° phase-shift delay-locked loop (DLL) contains new biased Delay Line Controller which consist of buffers, encoder to produce the delay code to control the delay line. The rest of this paper is organized as follows. A brief overview of previous DLLs is presented in Section II. In Section IV, the proposed Delay Line Controller is designed. Section V gives the proposed all-digital 90° phase-shift DLL. The experimental results of the proposed DLL are presented in Section VI. Section VII gives the conclusion of this work.

II. OVERVIEW OF PREVIOUS WORKS IN DLL

In previous DLL Architecture consist of Phase Detector, Charge Pump, DSLC,DLC and Delay line. The DSLC accepts several outputs from the PDDW and generates control signals for the delay-line controller. The DSLC consists of three blocks: 1) a sample and compare path (SCP); 2) a sample number counter (SNC); and 3) an optimization feedback loop (OFL). Because the DSLC performs signal processing with several outputs of the PDDW, it reduces the bandwidth of the DLL. As a result, the lock speed of the DLL can be degraded if the DSLC is enabled during the tracking mode. Thus, in the tracking mode of the DLL, the LOCK signal is LOW, and the outputs of the PDDW PDUP, PDDN, and PDHO*)* are directly applied to the delay-line controller via multiplexers (MUXs). After the DLL is locked, the SCP, SNC, and OFL operate to suppress dithering jitter. The PDDW before the SCP compares the phases of the input and output clocks of the DLL, CLK_{ref} and OUT_{ring}..

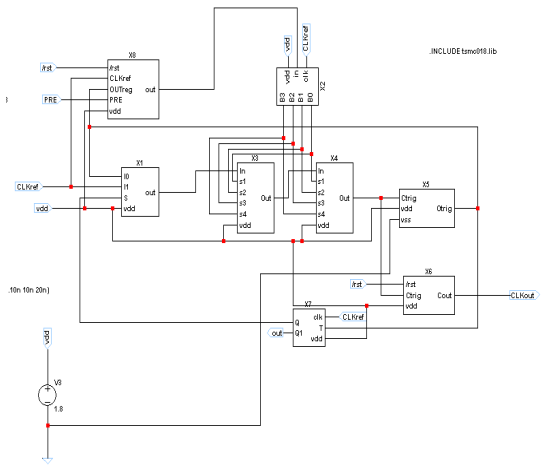


Fig.1. DLL Circuit in LT spice software.

The up and down signal is controlled through charge pump which generated control voltage. This voltage signal is given to Delay Line Controller. Then the output of DLC is used to control the delay line operations which generate the clock signal output.

The entire circuit is designed in LT spice software to analyze performance of each circuits through transient analysis. This make it possible to reach a high frequency operation. Bias circuit is used to give constant currents depend on Vcntrl which to varies time delay of each stage to minimize the phase error.

When DLL is in locked condition, the input and output of delay chain are inphase. Locking time refer to time interval for DLL takes to achieve a stable locking state from an initial state. So, the shortest locking time is required to achieve good performance of DLL.

The entire DLL circuits are designed in LT spice Software as shown in Fig.1. The parameters of DLL are Acquisition time: 19.95us, Capture range: 14-19.95us and Lock in range: 20-100us for this circuit.

III. Tanner EDA SOFTWARE

Tanner EDA provides a complete line of software solutions that catalyze innovation for the design, layout and verification of Analog and Mixed Signal (A/MS) integrated circuits (ICs). Customers are creating breakthrough applications in areas such as power management, displays and imaging, automotive, consumer electronics, life sciences, and RFdevices.

A low learning curve, high interoperability, and a powerful user interface improve design team productivity and enable a low total cost of ownership (TCO). Capability and performance are matched by low support requirements and high support capability as well as an ecosystem of partners that bring advanced capabilities to A/MS designs. Founded in 1988, Tanner EDA solutions deliver the right mixture of features, functionality and usability. Different Modules are used in tanner. They are S-Edit ,T-Spice ,W-Edit ,L-Edit and LVS.

In this Software, the circuits are designed in S-Edit Schematic Capture. Tanner S-Edit Schematic Capture increases the design productivity while handling the most complex IC designs. This powerful environment supports fast and cross-probing between schematic, layout and LVS reporting at net and device levels. Tanner Waveform Viewer (formerly known as W-Edit) provides an intuitive multiple-window, multiple-chart interface for easy viewing of waveforms and data in highly configurable formats.

IV.THE PROPOSED DELAY LINE CONTROLLER

Fig.3. shows the design considerations for the Delay Line Controller in the proposed structure [7]. The Delay Line Controller produces the delay code to control the delay of delay line. The Delay Line Controller of contain 15 sets of buffers, D-flip flops and 16:4 encoder. The 15 set of buffers are used to get 15 control signals. The control signals are passed through D-flip flops and then the output of flip flops are encoded into 4 bit control code in encoder.

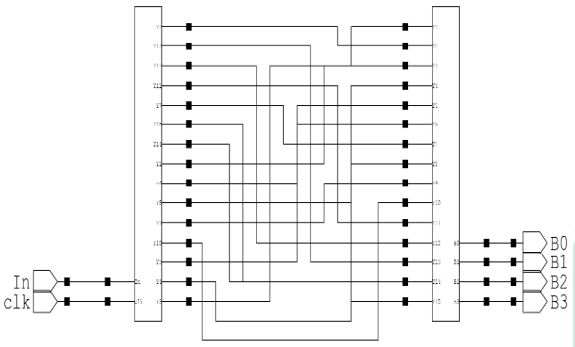


Fig.3. Structures of the Delay Line Controller

The output of D flip flop are given to the encoder circuit which encode the signals. In this structure , we are using 16:4 encoder. So finally gets the 4 bit delay code which is used to control the delay line circuits.

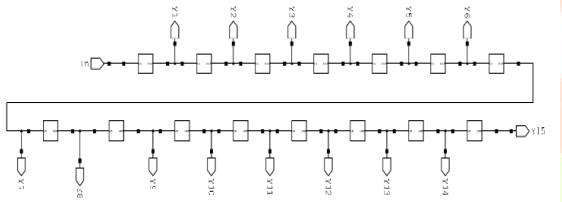


Fig.4. Structures of the Time delay unit in DLC.

The proposed all-digital 90° phase-shift DLL utilizes a sequential search scheme to obtain the control words, the lock time depends on the length of the delay line, and is exponentially proportionate to the number of control bits.

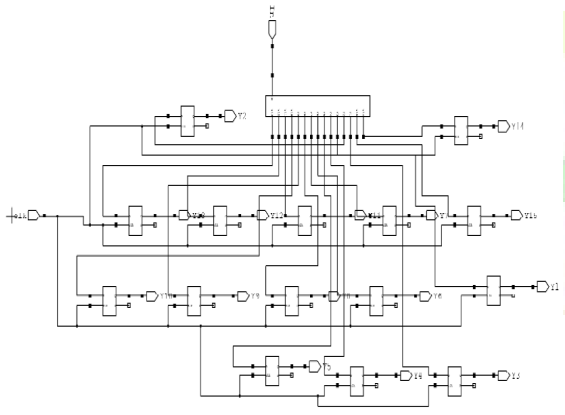


Fig.5. Structures of the Time delay unit with D-flip flop.

This delay codes are given to the selection codes of the delay line which control to reduce locking time and to prevent the harmonic locking problem.

V. ALL-DIGITAL 90° PHASE-SHIFT DLL

A. Overall Structure and Operation

Fig. 6. shows an overall block diagram of the proposed all-digital 90° phase-shift DLL based on a multiplying DLL (MDLL)-based structure [4] in which the delay line, MUX, and frequency divider dummy (FDD) form a ring oscillator. The multiplying factor of the proposed structure is fixed at two. The delay line consists of a NAND-gate-based ladder-type coarse delay line (CDL), as described in [8], and a fine delay range selector and resistance-controlled fine delay unit, as described in [1].

The ring oscillator is initialized to avoid delay error accumulation in the ring oscillator. The initialization is performed when the operation step changes and when the delay line controller changes the delay of the delay line to detect the phase alignment without the accumulated delay error caused by previous delay code. The delay code is adjusted to ensure two oscillator of the ring oscillator, it caused error in delay line.

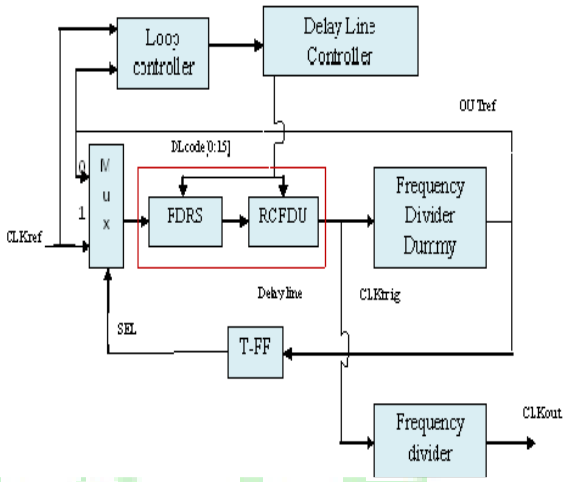


Fig.6. block diagram of the proposed all-digital 90° phase-shift DLL

The proposed DLL structurally resolves the delay-line mismatch problems in [5]–[9] by adopting an MDLL-based structure. The mismatch among the delay-line segments are structurally eliminated, and the additional buffers in [10] and [11] or the independent control loop for delay-line segments in [1] and [12] are no longer required. In this manner, the proposed DLL can attain a high 90° phase-shift accuracy with a large reduction in the core area and delay-line length.

B. Design Considerations and Circuit Details

A. Proposed PD with a symmetric detection window:

Dithering jitter is caused by the quantized delay step of the digitally controlled delay line. To reduce dithering jitter, a digital DLL using a phase detector (PD) with a detection window (PDDW). The PDDW has an additional output— the HOLD signal. If the timing skew of the input and output clocks of the DLL is less than the detection window, the PDDW generates HOLD instead of UP or DN and then disregards the timing skew. In this way, dithering jitter is suppressed.

Fig.7.shows the proposed symmetric window PD. Before the rising edges of IN_1 and IN_2 arrive, M1 and M2 are turned OFF, and UP and DN are precharged to HIGH. While the DLL is in the tracking mode, the LOCK signal is LOW, the cross-coupled inverter (CCI) configuration in Fig. 10(c) is connected, and the skewed buffer path is turned OFF.

When the rising edge of IN_1 (IN_2) arrives, M1 (M2) discharges the node UP (DN), after which the positive feedback characteristic of the CCI configuration quickly charges the node DN (UP) to HIGH and discharges the node UP (DN) to LOW. This CCI configuration keeps the detection window of the proposed PD in the tracking mode very small.

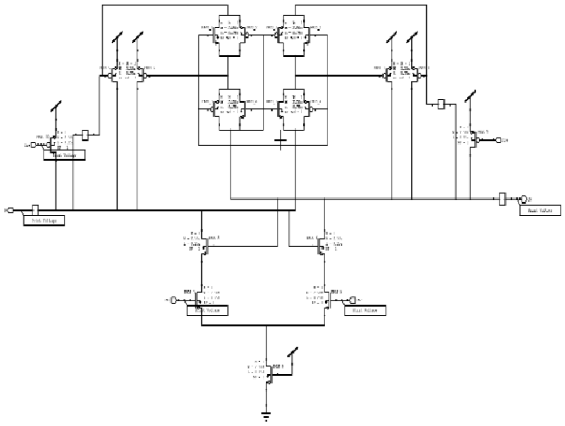


Fig.7. Proposed PD with a symmetric detection window

After the DLL is locked and enters into the steady-state mode, the CCI configuration is turned OFF, and the skewed buffer path is turned ON. As in tracking mode, when the rising edge of IN_1 (IN_2) arrives, M1 (M2) discharges the node UP (DN); however, the discharge operation occurs more slowly than that in the tracking mode because a positive feedback path does not exist in the skewed buffer path. If the rising edge of IN_2 (IN_1) arrives late, M4 (M3) is turned OFF, and as a result, DN (UP) remains HIGH, even after IN_2 (IN_1) arrives. However, if the rising edge of IN_2 (IN_1) arrives quickly, the node DN (UP) can be also discharged before M4 (M3) is turned OFF, following which both UP and DN become LOW. In this manner, the proposed PD forms the detection window. Unlike the PD in [1], the proposed PD operates identically for both the lead and lag cases of the two input clocks, thus forming a symmetric detection window.

B. Fine Delay Range Selector (FDRS):

As the operating frequency increases, the demanded delay resolution of an FDU becomes finer to achieve an accurate phase alignment in fig.8. The proposed AD-90 DLL also suffers this problem because the delay change is accumulated four times during two oscillations of the ring oscillator. Thus, the fine delay resolution must be lower than one fourth of the phase detection window of the PD to lock the 90 phase shift. However, this finer delay resolution means that a greater number of FDUs are required to cover the delay of the signal.

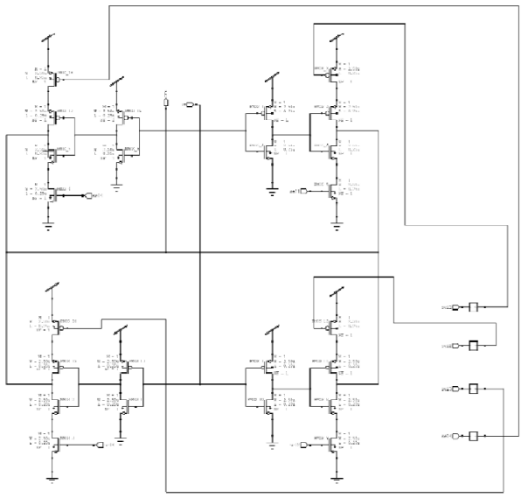


Fig.8. FDRS circuitry.

Thus, the maximum operating frequency of the DLL decreases with the finer delay resolution because of the delay increase in a FDL. This FDRS consists of four buffers constructed by different Devices which are differentiated from different width and length of the transistors.

C. Resistance Controlled Fine Delay Unit (RCFDU):

An inverter is used as the delay unit of a PD to achieve a narrow phase detection window. The RCFDU consists of two inverters and transmission gates that are connected in parallel as shown in fig.9. Because a transmission gate can be modelled by a resistor, a switch, and a capacitor, the equivalent circuitry of the RCFDU. The resistors correspond to the turn-on resistance of the transmission gates and

the capacitors (C1 and C2) correspond to the summation of the junction capacitances of the transmission gates.

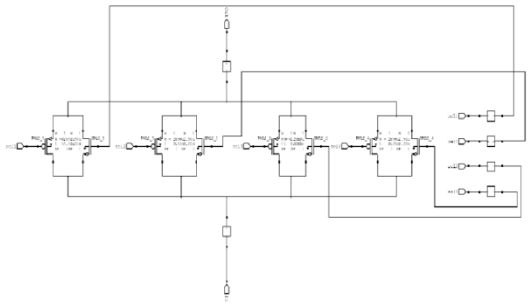


Fig.9. RCFDU circuitry

The effect of the variations of C1 and C2 caused by the change of junction capacitances according to the control code *sel*[0:3 and */sel*[0:3] , on the delay variation can be neglected, because the small transistors whose capacitances are small are used, as shown in Table I.

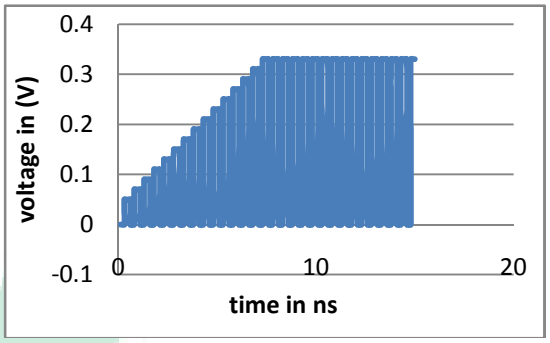
TABLE I
SIZES OF TRANSMISSION GATES

	W1	W2	W3	W4
PMOS	270n	280n	290n	300n
NMOS	135n	140n	145n	150n

However, the change in the effective resistance is relatively large according to the control code. This changes the *RC* time, which directly affects the signal slope at node A. Thus, the delay of the RCFDU can be controlled by the control code. The delay resolution of the RCFDU can be easily adjusted by transistor sizing. Four transmission gates are used in this paper, and they are scrupulously sized to achieve a finer delay resolution.

VI. EXPERIMENTAL RESULTS

The output signals of delay line is passed to the frequency divider and then frequency divider is



Simulation output of all-digital 90° phase-shift DLL

used to generate the output clock signal. The output is gradually increased and stable at one state, that particular state is called lock in range. The simulated output of all-digital 90° phase-shift DLL is shown in fig.10.

Table II summarizes the performance of the proposed 90 ° phase-shifts DLL and provides a comparison with previous schemes. The operating frequency range of the proposed DLL is from 400 to 800 MHz Because the proposed structure adopts MDLL structure with multiplying factor of 2, the rising edge of CLK_{ref} propagates through the ring oscillator four times in one period of CLK_{ref} ,

TABLE II

COMPARISONS OF VARIOUS TECHNIQUES

	Method	Extra hardware	Features
[5]	Replica delay line	1 delay cell. Current-steering PD, higher-order loop-filter	Larger area, duty cycle of the signal must be 50%
[9]	Self-correcting	Lock detector	Larger area, duty cycle of the signal must be 50%
[10]	PD with reset circuitry	8MOS	Static PD, higher reset path, lower speed
[11]	Stage selector	1VCDL	Large area
Proposed	TDC Based Delay Line Controller	15 DFF	Reduce delay error, smaller area, higher speed

The reduction in the delay-line length and the absence of additional calibration circuits compared with the structures in [1] and [5], the core area and power consumption of the proposed structure are reduced by more than 66% and 60%, respectively.

Layouts are drawn using TANNER and electrical tools. In Tanner EDA Software, the layout of the DLL circuit is generated through L-Edit Module. This layout is used to fabricate the DLL in DRAM. The operating frequency is also increased with synchronous structure.

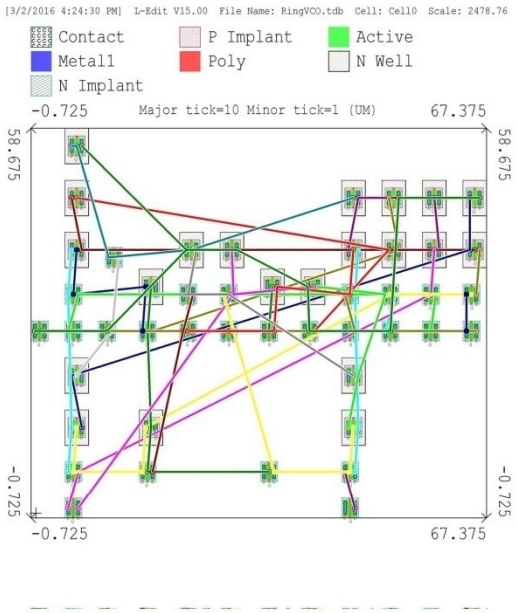


Fig.11.Layout of TDC in DLL

The design of a Low Power CMOS Delay Locked Loop with lowest power consumption has been implemented. Various circuit and architecture parameter tradeoffs are evaluated. This architecture has a large degree of flexibility in design.

VII. CONCLUSION

An area- and power-efficient 90° phase-shift ADDLL with a duty-cycle correction function and a Delay Line Controller is dealt in this paper. The ADDLL alleviates the delay-line mismatch issues observed in DLL structures and reduces the length of the delay line by a factor of four by adopting an MDLL-based structure. The absence of an additional delay line for duty cycle correction and additional calibration circuits for delay-line mismatch enable a reduced power consumption of 10.2 mW. In addition, a fast operating frequency with finer delay resolution is obtained from the FDRS and RCFDU. The simulation results show that the Low Power CMOS Delay Locked Loop is preferable for the next generation deep sub-micron low voltage CMOS DLL. The implementation of AD-90 matches well with future technology trends such as technology scaling, low supply voltage, and high frequency, allowing it to be usefully applied to future circuit systems.

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