LOW POWER AND HIGH SPEED PARALLEL TEST ACCESS MECHANISM TECHNIQUE BASED MULTICORE TESTING ARCHITECTURE

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Abstract- *Embedded cores are now commonly used in large system-on-chip (SOC) designs. However, through chip inputs and outputs embedded cores are not accessed directly, so special access mechanisms are required to test them at the system level. In the proposed approach test access mechanism (TAM), provides the mean for on-chip test data transport. This method is to design the low-power scan chain based parallel multi core testing architecture. The architecture consists of different internal core architecture and to identify the faulty circuit using string conversion technique. The scan chain process is used to analyze the separate core internal architecture output values. This paper demonstrates the simulation results and comparison table indicating the test pattern generation and compression using Xilinx software tool.*

Index terms- System-on-chip (Soc), Test-Access-Mechanism (TAM), Multi core Testing Architecture.

I. INTRODUCTION

A. System-On-Chip:

System-on-chip (SOC) is designed based on reusable intellectual property (IP) cores. SOCs can reduce manufacture cost and offer rapid system implementation. However, the testing for SOC has become a significant and serious challenge. To simplify complexity of test access and application the modular test of the IP cores in an SOC is utilized frequently. In modular test, core test wrapper isolates an embedded core from its environment, and test access mechanism (TAM) which facilitates modular testing is developed to transport test data from the SOC pins to core terminals. SOC test techniques requires specialized hardware infrastructure such as TAM and test wrappers.

C. Test Access Mechanism:

Many system-on-chip (SoC) integrated circuits today contain multiple hierarchy levels for both design and test. TAM technique avoids wasting excess free variables and improves the compression ratio of SOC testing. Consequently, it can help with controlling the SOC test cost. TAM technique is applied to deliver test vectors from the source to CUT.

The main function of TAM is to transport test responses from the CUT to the test sink. TAM design involves making tradeoff, data transport capacity, test time and TAM overhead. Cores using the same TAM lines are tested sequentially unless their test patterns are compatible, while those using the different TAM lines can be tested in parallel. Compressed test data is delivered from tester via TAM to linear decompressor in the cores. Then the test patterns decompressed by linear decompressor are shifted into scan chains in cores. To guarantee the compressibility of each test cubes for a single core, the number of free variables of the linear decompressor should be set according to the largest number of care bits in a test cube. We present two approaches for efficient testing of SoCs with hierarchical cores. In the first approach, a conventional wrapper design is used which gives flexibility for TAM optimization and test scheduling. In the second approach, for testing of parent and child cores a modified wrapper design is used. This achievement can be attributed to advances in semiconductor process technology and it provides high performance, low power, and short time-to-market.

II. RELATED WORK

A novel method for statistically encoding test vectors for full-scan circuits using selective Huffman coding is presented in [7]. The deterministic test vector compression technique for SoCs using block matching has been presented in [1].A scheme for compression and decompression of test data using cyclical scan chain is presented in [2]. A professional approach for compressing test data using run-length coding and Burrows–Wheeler transformation (BWT) is existing in [3]. The BIST scheme for non scan circuits based on statistical coding using comma codes and run-length coding is described in Iyengar *et al.* [4]. A test data compression technique using dictionary-based and bitmask selection criteria was proposed by Basu and Mishra [5]. The bitmask-based compression technique [5] is developed to deal with the mismatch problem of the dictionary-based technique by generating more matching patterns. But, the procedure is unable to handle the data set containing don't care values. A different technique for test data compression/ decompression has been proposed in [6]. It has achieved higher level of compression but it needs extra on-chip hardware and extreme power consumption and time.

III. PROPOSED SYSTEM

This technique is used to test the all internal core architecture for parallel form. This work is to implement the test pattern creation and to apply the scan chain process. This process is to analysis the separate core internal architecture output result values and fault identification comparison process between expected test response and present test response results. The cores using the exact same TAM lines are divided into a group. Cores in the same group are tested sequentially unless their test patterns are compatible. Those using not identical TAM lines can be tested in parallel. Compressed test data is delivered from tester via TAM and decompressed in the cores by linear decompressor. Then the decompressed test patterns are scanned into scan chains in cores. This paper presents a hybrid test vector compression method for very large scale integration (VLSI) circuit testing, targeting on embedded cores-based SoCs. In the proposed approach, a software program is loaded to the on-chip processor memory with the compressed test data sets. The developed scheme requires minimum hardware overhead based on on-chip embedded processor can be reused for normal operation. One of the test vectors is considered as reference test vector and the subsequent test vector is generated from the previous vector by storing only those blocks that differ from the previous one. This is a faster procedure since the number of operations is much less because of merging was carried out without delay from the reduction of the set of blocks. The advantage of this system is to improve the TAM system performance level and reduce the power consumption level. It is used to increase the test pattern generation process and reduce overall circuit complexity level. It provides high reliability.

BLOCK DIAGRAM

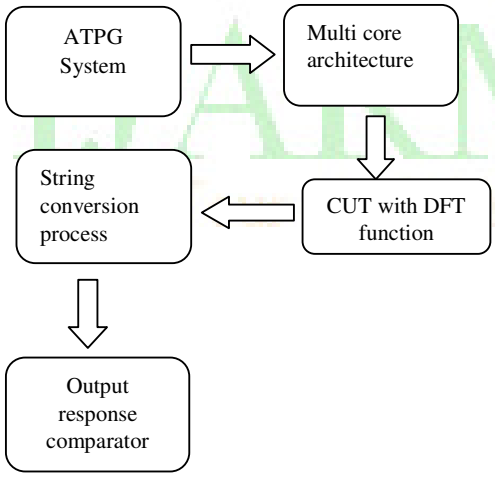

Fig.1. Block Diagram

MODULE DESCRIPTION

A. ATPG GENERATION

This work is mainly based on automatic different core testing process using reset and clocking sequence. The pseudo random pattern generation process is mainly used to generate the pattern results based on normalized Euclidean distance. LFSR consist of D-FF connected in cascade with the same clock applied to the entire FF to make them act like a shift register. This XOR operation introduces a new bit into the shift register. ATPG (Automatic Test Pattern Generation /Generator) is an electronic design automation technology used to find an input sequence that applied to a digital circuit and it enables automatic test equipment to distinguish between behavior of the correct circuit and the faulty circuit. These patterns are used to test semiconductor devices after manufacture, and in some cases to assist by determining the failure analysis. These metrics generally indicate test quality and test application time.

B. MUTICORE ARCHITECTURE

Our process considers the arithmetic core architecture. It consists of adder, comparator, subtractor, multiplier architecture. This architecture consists of more number of gate components, so it has more chance to error occurs in output results. So every time we analysis the circuit activation process and to detect the error occurrence in multi core architecture.

C. CUT WITH DFT FUNCTION

Our circuit under test function is considering the different arithmetical core architecture. These architectures are produce the 16 bit output result in each process. Circuit under test was performed before the device assembly. The results in prevention of circuit and device and also the fault detected at this stage results less cost than the fault identified at device level. Our work is to identify the faulty circuit effectively and separately in multi core architecture. This architecture is to modify the testing methodology using majority logic function.

D. STRING CONVERSION PROCESS

Our work is to get the 16-bit output test data bits and to apply the string test data conversion process. So we split the 16-bit into 8-bit LSB and 8-bit MSB data test bits and to apply the ASCII string code. This compressed string output test bits is to optimize the overall multi core circuit testing process and to improve the system accuracy level. The Burrows–Wheeler transform (also called block-sorting compression) rearranges a character string into runs of similar characters. This improves the efficiency of compression algorithms, but requires extra computation. When a character string is transformed by the BWT, the transformation permutes the order of the characters.

Steps Followed in Compression

a. Division of Test Data into Blocks

The pseudo random pattern generation process is mainly used to generate the pattern results based on normalized Euclidean distance. LFSR consist of D-FF connected in cascade with the same clock applied to the entire FF to make them act like a shift register. This XOR operation introduces a new bit into the shift register. All the test vectors are divided into number of blocks of equal size. The size of a single block depends upon the total number of bits in each vector. One of the test vectors is considered as a reference test vector and the next vector is generated from the previous vector by storing only which block that differ from the previous one.

b. Frequency Computation of Data Blocks

After completing this block matching process, the high frequency and low frequency blocks are separated for further process. There will be lots of unspecified data that is denoted by x. The frequency of a block depends on the number of unspecified data in the blocks. All the blocks having those minterms must be removed from the list of data blocks that is used to calculate the frequency of another block. There exist several algorithms to fill the unspecified data fields with 1 s or 0 s. In an efficient algorithm described in [13], initially most repeatedly occurring unspecified block is determined. Then, it is compared with the next most repeatedly occurring unspecified block to see if there is a difference in any bit position. If there is no difference, then they are merged with the specified value. This is the faster procedure and the number of operations is much less.

d. Preprocessing of High Frequency Data Blocks and Application of Various Coding Techniques

The BWT algorithm is executed on all high frequency blocks of data. The Burrows and Wheeler transform is a block sorting lossless and reversible data transform. The BWT can transform a text into a new sequence which is usually more "compressible". The transformed text can be enhanced with fast locally-adaptive algorithms, such as run-length-encoding or move-to-front coding in combination with Huffman coding or arithmetic coding. This transformation takes a block of data and rearranges them using a sorting algorithm known as lexicographical sorting. The original ordering of the data elements can be restored with no loss of fidelity.

Finally, the individual coding techniques such as Huffman coding, Golomb coding, LZW coding, and ACB are employed, for efficient compression.

E. OUTPUT RESPONSE COMPARATOR

The final output is to identify multi core arithmetic operator circuit the fault effectively and to reduce the test process time. The output response comparator process and it compare the golden signature from ROM memory and present signature level. This proposed majority based multi core circuit scheme is to identify the fault effectively and to reduce the power consumption level due to the testing.

IV.PERFORMANCE ANALYSIS

Xilinx ISE[1] (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs which enable us to compile the designs, perform timing analysis, examine RTL diagrams, simulate a different stimuli, and configure the target device with the programmer. To get fine result this technique is implemented in VHDL language. The percentage data compression was computed as follows:

$$\%\text{Compression} = \frac{(Original\_Bits)-(Compressed\_Bits)}{Original\_Bits} \times 100. \quad (1)$$

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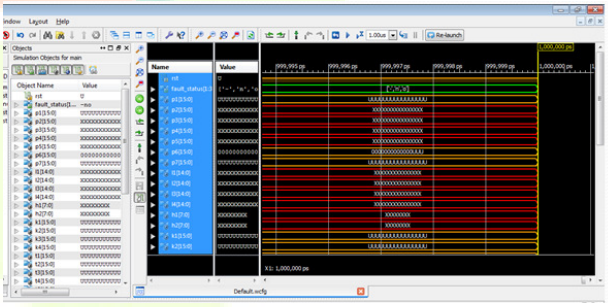

Fig.2 Input Initialization.

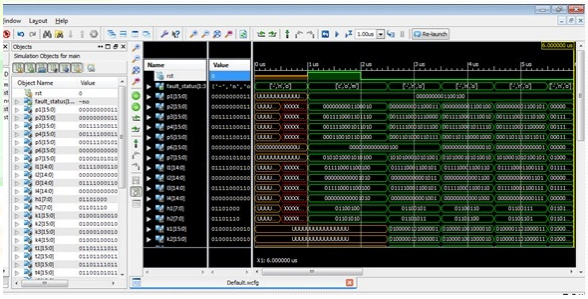

Fig.3 Output Response.

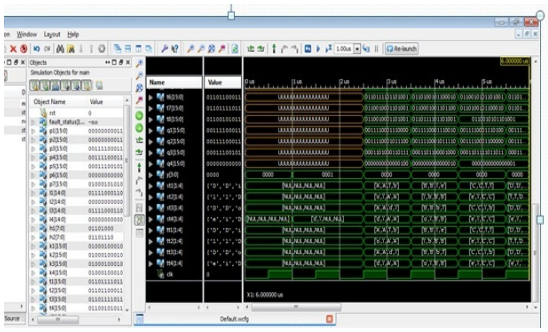

Fig. 4 String Conversion Process.

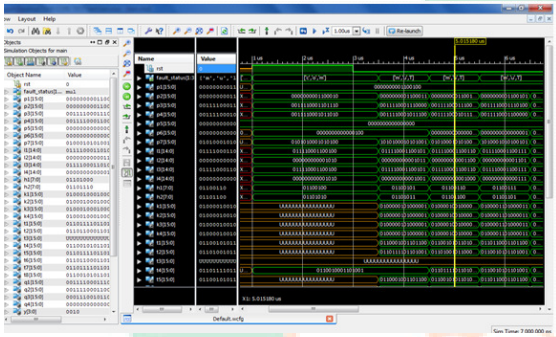

Fig.5. Fault detection process.

In Fig.2. Initialization is performed using clock and reset switches. Output response of this process is described in Fig.3. It shows the compressed test vectors which have low and high frequency data sets. The string conversion process is demonstrated in Fig.4. In this the compressed test vectors converted into string using string conversion process. This compressed string output test bits is to optimize the overall multi core circuit testing process Fig.5. Shows the fault detection process where present signature and golden signature is compared using output response comparator. It improves the system accuracy level.

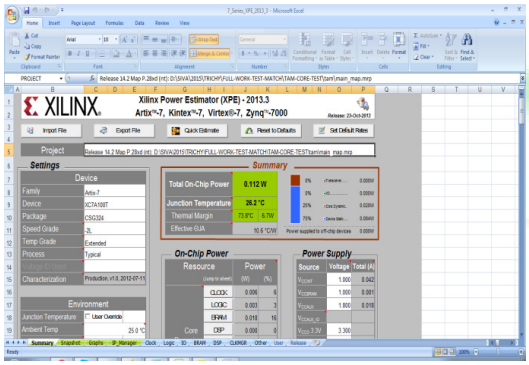

Fig.6. Power Consumption Report.

It shows the power consumption report of this compression process.

COMPRESSION CALCULATION:

= (32 – 4) / (32) * (100) = 87.5%

From these results, it is clear that the developed compression strategy provides better compression results than the other compression methods.

V.CONCLUSION

Finally we design the low-power scan chain based parallel multi core testing architecture. This architecture consists of different core architecture and identifies the faulty circuit using string conversion technique compared to existing methodology. By sharing free variables between cores tested simultaneously in SOC, the proposed SOC test technique provides greater flexibility in test compression. It does not have detrimental effects on an additional area and potential performance overhead.

The proposed scheme can also be expanded by sharing common channels among three or more core groups to obtain better results. This technique can be extended by using the 16 bit majority architecture for data encoding process and to modify the majority function using the Boolean logic function. This logic function optimizes the Boolean equation where it reduces the gate component for the 16 bit majority architecture.

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