A 14-GS/s, 3-bit, At-speed Testable ADC and DAC Pair in 0.18μm CMOS

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***Abstract*— This paper demonstrates a 14-GS/s 3-bit Flash Analog to Digital Converter(ADC) and Digital to Analog Converter(DAC) pair in 0.18μm CMOS for the design of advanced serial-link transceivers. Current mode logic (CML) gates which is mainly meant to achieve high speed and to avoid the severe power bouncing issues are replaced by Complementary Pass Transistor Logic (CPL) to achieve low power . The active feedback amplifiers and CPL logic are responsible for achieving the ultimate 14 GHz sampling rate. A design-for-testability circuit using the digital loop-back are added to conduct the at-speed tests by internally cascading the ADC and DAC. Design-for-testability(DFT) circuits are added by internally cascading the ADC and DAC has two modes for conducting the at-speed tests. The ADC and DAC consumes 620 mW and 110 mW from a 1.8-V supply, respectively. This paper also involves with INL and DNL calculation of ADC and DAC.**

***Index Terms*-Flash ADC, DAC, DFT ,GS/s**

I INTRODUCTION

High speed data converters are advantageous for upcoming real time applications like software defined radio, UWB ,disk read systems, radars and instruments. In specific, the applications which involves optical or wired serial links prefer data converters that has a high sampling rate and a dynamic range which can lead to increase in data rate and reduction in the Channel Bandwidth Requirement. There are ultra-high speed data converters which still uses using GaAs or SiGe technology [1], [2]. But, they consume more watts. In particular, if the data converters were realized and implemented with standard CMOS processes then integrating with the exile and powerful digital circuits becomes possible. Recently, several very high speed Flash CMOS ADC designs have been published [3], [4] which shows that by using 0.18 μm or advanced CMOS technology, it becomes possible to achieve a sampling rate higher than 10 GS/s with significant reduction in power consumption. This paper demonstrates a fully integrated, non-interleaved, 14-GS/s, 3-bit ADC and DAC pair in 0.18 μm CMOS technology. Sec. II describes the circuit design and indicates the design challenges. The current mode logic circuits are replaced by complementary Pass Transistor logic to make the data converters low-power, very fast, and having less noise. A test circuit has been designed to enable the testing of the Data Converter to make it available to operate in two testing modes. Sec. III shows the final conclusion

II CIRCUIT DESCRIPTION

The simplified block diagram of the Data converter pair is shown in Fig.1.The Flash ADC and the DAC acts as the record holders of the highest sampling rate data converters that increases the overall channel capacity which in turn increases the resolution [5]. In addition, a design-for-testability block for at-speed tests was added to the data converter pair in order to address the difficulty in testing. All circuits including the analog and logic parts are realized using fully-differential structures for alleviating the common-mode interference and noise.

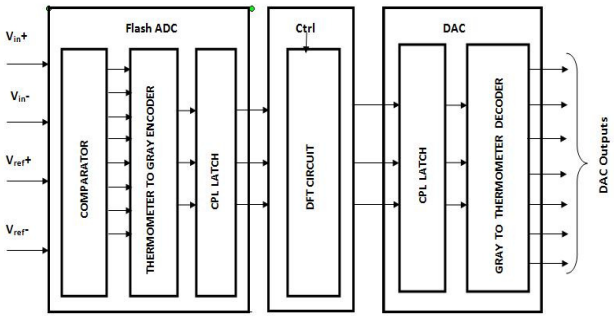

Fig. 1. Block diagram of the Data converter pair

2.1. FLASH ADC

Depending on the application used ,numerous ADC architectures are available ranging from high-speed, low resolution flash converter to the high-resolution, low-

bandwidth oversample noise-shaping sigma delta converters. The architectures which are meant for high-sample rate applications, either in a single-channel or time-interleaved are:

- Flash ADCs – It is a parallel converter architecture. The entire conversion is made within one clock cycle.
- Folding ADCs – These are flash ADCs with added multistep implementation. The conversion is made within one clock cycle.
- Pipeline ADCs –Pipeline has numerous stages, which achieves high throughput at the cost of increased latency while allowing more efficient implementations for medium resolutions.

• Successive approximation ADCs – This architecture generates one bit per clock cycle. Low area needed for the comparator becomes the prominent one as comparator is the implementation is the beneficial one of this structure. For resolutions below 3 effective bits and sample rates up to 14 GS/s, flash ADCs are the most common architecture preferred compared to other architectures[11].

The Flash ADC architecture that contains the highest potential single-channel sample rate of all the architectures contains the components such as resistor ladder structure, the comparator structure and the Thermometer to Gray Encoder as shown in Fig.2.

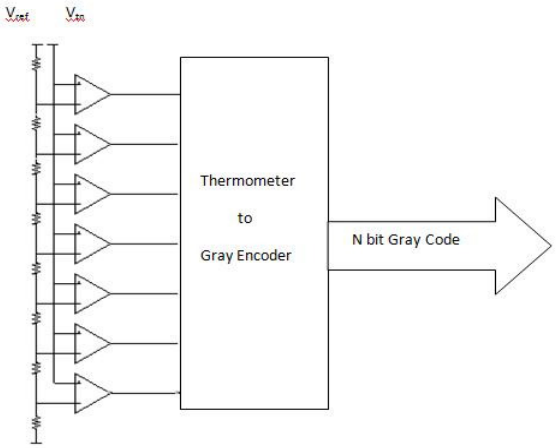

Fig.2.Flash ADC Architecture

The parallel comparison contained in the circuit having the input signal to the 2n -1 reference levels is the decision made by the correct quantization level. In Flash ADC ,the reference voltage is generated by a resistor ladder having 2n equal resistance of 1KΩ.The comparator compares the input voltage level with the reference voltage level, which produces the equivalent thermometer coded output in the digitalized form. In the Thermometer to Gray code converter that is used in Flash ADC , the‗1' -to- '0' transition level indicates the quantization level that corresponds to the input signal. To convert the thermometer code produced to an n-bit digital output , a Thermometer to Gray code converter is employed. Flash type ADC's is used in low latency targeted for real time applications like applications involving control loops .

2.1.1 COMPARATORS : In comparison with other ADC architectures , the Flash Architecture having number of parallel comparators is expected to offer a high input capacitance which makes it suitable for higher demands on the driver circuit. The Comparator is involved in the process of conversion from analog signals to digital signals. In the process of A/D conversion, sampling the input first becomes the predominant step. This sampled signal is then applied to comparators for further processing to determine the digital equivalent of the analog signal and it compare the analog signal with another reference signal and outputs are binary signal based on the comparison. In the front-end of a radio-frequency receiver, Low power and high speed ADCs are the key ingredients available in most of the modem telecommunication systems. The optimization of the heart of the Data Converter which plays a main role in limiting the speed of the converter. utmost importance. In a flash ADC, the offset of the individual comparators in the array will degrade the overall linearity and causes further reduction in Signal to Noise Distortion Ratio.

So in order to have low offset, the comparators has to add cascaded stages of preamplifier [6]which leads to increase in size of the comparator. Only then the trade-off between speed and power can be achieved at the cost of sufficient low offsets. Depending on the requirements of speed, offset, noise and power dissipation, different comparator topologies exist .The basic components of a comparator consist of a latch and a pre-amplifier and double ended fully differential Amplifier, with a more complex comparator as shown in Fig.3.Here the latch preferred uses CPL Logic against the CML Logic stated in [1].

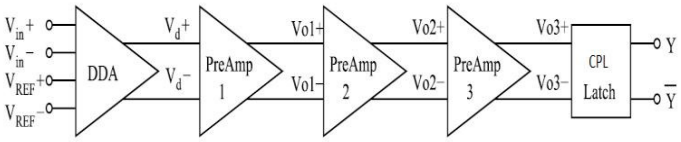

Fig.3.Block Diagram of comparator

The Comparator used here involves the fully differential input structure. The main reason for choosing the Fully differential input structure is it provides maximum noise rejection.

A. DDA : The fully differential input structure preferred here is DDA. The DDA is different from the Preamplifier stage used as because of its selected gain which is close to unity and its information measure makes its way contributing to the specification of the comparator. Fig.4 shows the schematic of DDA. The amplified version of the first differential input voltage is generated in accordance with the differential reference voltage. The DDA style contributes pairing of the positive input and also the positive reference in spite of the negative input. Such an arrangement avoids keeping the differential try functioning with a differential reference input as high as 800 mV. For acceptable dynamic common-mode rejection, the differential architecture is used in conjunction with acceptable input bandwidth in the Track and Hold circuit. It is made possible that coupled-noise may cause the differential inputs to exceed the ADC's allowable input voltage range in case of noisy environment. The input voltage range is minimized in such a way that the ADC input range shouldn't exceed in order to achieve best performance. The differential signals are also meant for increasing dynamic range which is an additional key feature for the Flash ADC. Since the power supply drops with the upcoming technology, the design engineers are looking for ways to offer greater input dynamic range.SNR increases with superior DC and AC common-mode rejection(which manifest themselves as noise) as the fully-differential inputs have 2 times the full-scale input voltage level. Hence the DDA with fully differential input structure is

used in the comparator as shown in Fig.4.The Double Differential Amplifier has four inputs namely $V_{in}+$,$V_{in}-$, $V_{ref}+$ and $V_{ref}-$ as shown in Fig.3.

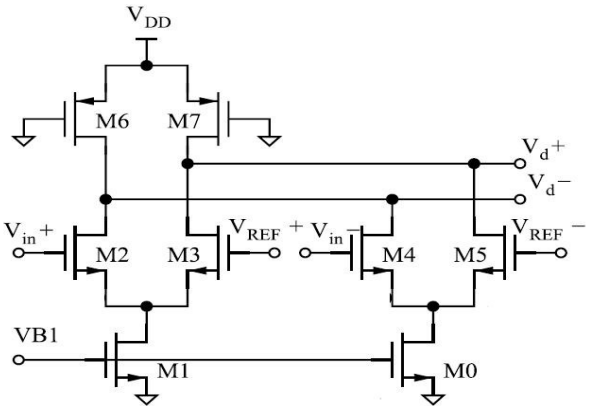

Fig.4. Circuit for Double Differential Amplifier

The Double Differential Amplifier achieves a gain of 1.84dB as shown in Fig.5.

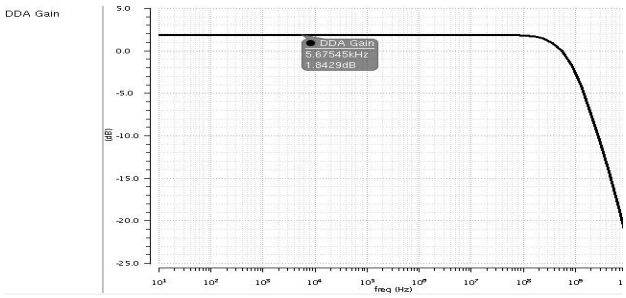

Fig.5.AC Simulation Result for DDA

B. PREAMPLIFIER : The preamplifier stage shown in Fig 6 is used for amplification of the input signal in order to achieve better comparator sensitivity i.e. the comparator can make a decision with increase in the minimum input voltage and can isolate the comparator from switching noise resulting from positive feedback stage based on those decision .The Preamplifier is nothing but differential amplifier with active loads.

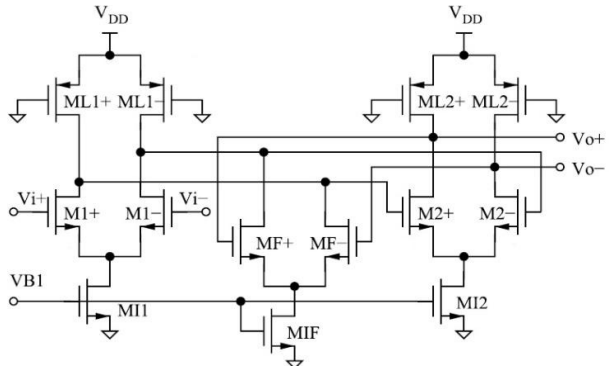

Fig.6. Circuit for Preamplifier

The preamplifier working as a transconductor will offer a current imbalance and trip the latch in either direction while entering the evaluation phase,. The latch with positive feedback is responsible for regenerating the nodes to full swing. The preamplifier thus designed achieves gain of 9dB as shown in Fig.7.

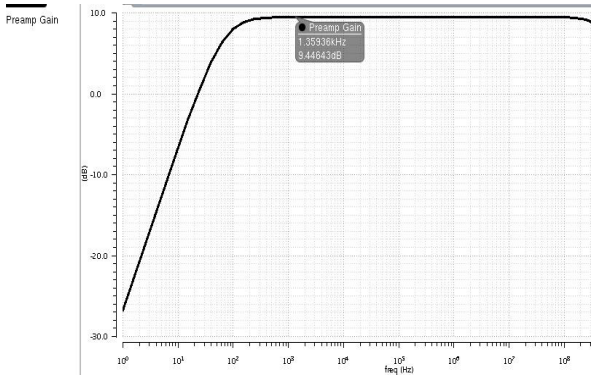

Fig.7.AC Simulation Result of Preamplifier

C. LATCH : The latch stage is used for determining whether the input signals is larger and making their difference to be amplified. In the reset-phase, the latch is either biased around the trip-point or pre-charged to a supply rail. The latch used here uses Complementary Pass Transistor logic in order to achieve low power.

Complementary pass-transistor logic is a combination of complementary inputs/outputs, a NMOS pass-transistor network, and CMOS output inverters. The circuit function is made possible for implementation in the form of tree which comprised of pull-up and pull-down branches. Since the threshold voltage drop of NMOS transistor degrades the ―high level of pass-transistor output nodes, the output signals are restored by CMOS inverters. CPL has traditionally been applied to the arithmetic building blocks and has been shown to result in high-speed operation [13],[14] due to its low input capacitance and reduced transistor count.

A general method of Karnaugh map coverage and mapping into circuit realizations is applied to design logic AND/NAND, OR/NOR, and XOR/XNOR gates in CPL. The method consists of the implementation of the gates from Karnaugh maps, and further simplifications: complementarily and duality principles which generates the entire set of two-input and three-input logic gates. The rules for Karnaugh map coverage and circuit realization of the CPL OR and CPL Latch as given below:

1. Cover Karnaugh-map with largest possible cubes (overlapping allowed).
2. Derive the value of a function in each cube in terms of input signals.
3. Assign one branch of transistor(s) to each of the cubes and connect all branches to one common node, which is the output of NMOS pass-transistor network.

Following the rules mentioned, the CPL Latch and the CPL OR gate is designed as shown in the Fig.8.

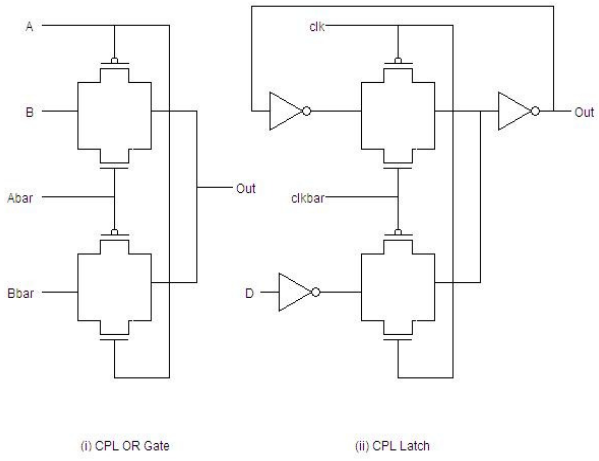

Fig.8. CPL (i) OR Gate (ii) Latch

The basic properties of the gates contribute to the generation of complementary principle. The complementary logic function can be obtained from the same circuit structure by applying the complementary principle. In complementary principle, the same circuit topology with inverted pass signals is capable of producing the complementary logic function in CPL. The complementarity principle holds in the targeted CPL logic as the pass variables directly pass on from the inputs to the outputs, making an inversion of the pass variables giving its complementary function.

TABLE I
POWER ANALYSIS FOR CML VERSUS CPL

Gate type		CML	CPL
OR	Power	4.83 W	
XNOR	Power		3.359 W
XOR	Power	6.26 W	3.685 W
LATCH	Power	8.80 W	4.63 W

The CPL logic thus used can contribute to low power which is clearly evident from Table I. Summing up, the latched comparator meant primarily for the clock signal related circuits indicates digital output voltage indicate whether the differential input voltage is positive or negative. A positive feedback mechanism that regenerates the analog input signal into a full scale digital signal is been faster and power efficient while performing multi-stage linear applications. The preamplifier latch comparator that is a combination of an amplifier and a latch comparator achieves high speed and low power dissipation. The amplifier meant for reducing offset voltage is added before the latch in order to achieve a high resolution. Thus, by considering factors of speed and resolution, preamplifier latch comparator are the choice for a high speed ADC. This type of latched comparator can be preferred in case of high speed and low power performance. By doing AC Analysis, the comparator is found to achieve a gain of 30dB as shown in Fig.9.

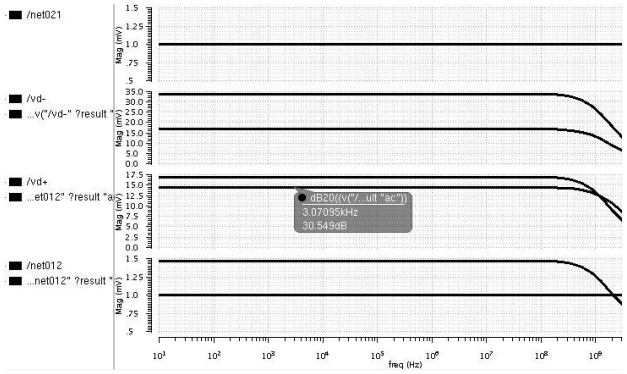

Fig.9.AC Simulation Result of Comparator

Input-offset voltage is a notable parameter in case of comparator. Large input-offset voltages are not acceptable in case of applications that involves high resolution converters. The circuit topology is not only meant for achieving low power dissipation but also for improving kickback noise and reducing the clock driving requirement. The speed of the comparator is an important parameter needed for analysis as the speed depends on both the initial voltage level of the latch during the beginning of the regeneration as well as the regeneration time constant ,which is given by

=

where ,C is the capacitance of the regenerative nodes and

is the total transconductance of the latch.

The regeneration time constant depends mainly on the transit frequency, f_T of the process but subjected to flaws by the relative size of the latch to the load as well as the bias conditions of the active transistors. Biasing the latch around the trip-point will lead to a fast decision time, whereas precharging the nodes to the supply voltage could reduce the power dissipation at the reset phase by persistently slowing down the decision time. A High sample rate can be achieved by cascading several preamplifier stages followed by clocked latches that makes an effective increase in the decision time affecting the additional latency. Hence this type of latched comparators can be preferred only in Flash ADC‘s and Folding ADC‘s and avoided from being used in Pipeline and SAR ADC‘s.

The random and systematic variations of the device parameters are the main cause of offsets. Latches are sensitive to variations and can even have high offsets. The variations in the device and the mismatch are likely to have an equivalent input difference, the offset voltage which must be applied in order to overcome this mismatch and bring the comparator to a metastable state. The mismatch occurs due to the threshold voltage variations in the input pair as well as the latching transistors, width and length variations of the

same and also capacitive imbalance of the internal and output nodes. Capacitive imbalance occurs if the voltage slope for equal input current and its feed-through is different i.e the clock signal produces different transient magnitudes. As the offset in a latch is large for small devices, Preamplifiers can be preferred for lowering the input referred offset, which can further be scaled by the Preamplifier gain thus reaching the low offset levels.

The Noise is linearly related to the function of the node capacitances. Similar to the case of the noise of a sampling switch, the transistor sizes has an impact on both the power spectral density of the noise as well as the bandwidth. However the node capacitances can limit the bandwidth and determine the noise level. The relative transistor sizes have an impact on the noise but for a standard sized comparator for which the result is close to 3kT/C. Similar to Offset, using preamplifiers will suppress the noise [12] of the later stages when referring this to the input.

C. ENCODER : A new improved multiplexer based encoder for flash analog-to-digital converter is proposed, which converts Thermometer code to Gray code as shown in Fig.10.

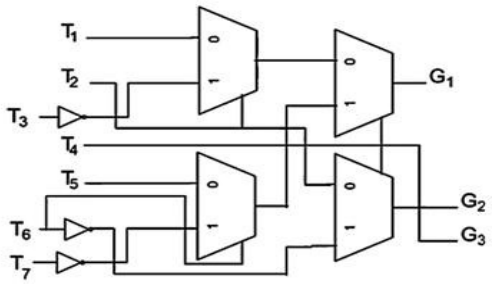

Fig.10.Thermometer to Gray Encoder

The functionality verification table of Thermometer to Gray encoder which is depicted in Table II.

TABLE II

FUNCTIONAL VERIFICATION OF THERMOMETER TO GRAY ENCODER

THERMOMETER CODE							GRAY CODE		
T_7	T_6	T_5	T_4	T_3	T_2	T_1	G_2	G_1	G_0
1	1	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	0
0	0	0	0	1	1	1	0	1	0
0	0	0	0	0	1	1	0	1	1
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	0

It can be configured to operate on Thermometer code with reduced length without any extra overhead which is suitable for adaptive resolution analog to digital converters thus resulting in better performance when compared to the existing encoders in terms of power, delay, area and figure of merit. The Thermometer to Gray encoder produces an outcome as shown in Fig.11.

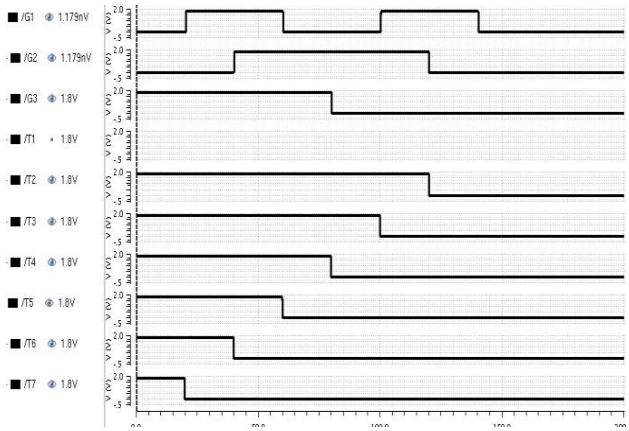

Fig.11.Transient Response of Thermometer to Gray Encoder

Thus the Flash ADC which comprises of components such as latched comparator, resistor ladder and thermometer to gray encoder produces a waveform as shown in Fig.12.

The transition of output code from —1 to —0 denote the input signal voltage level because the reference voltage are arranged increasingly from the bottom to the top of comparators array, the output code will all be equal to —1 as the reference voltage is lower than input voltage level and all —0 as reference voltage is higher than input voltage level which makes the output of Analog to Digital Converter look like thermometer code. The outcome from the comparator resembles a thermometer code and hence the encoder used is Thermometer o Gray Encoder which produces digitalized Gray coded outputs corresponding to the digitalized thermometer code obtained from the comparator earlier. Thus the final outcome of the Flash ADC will be a gray coded digital output as shown in Fig.11.

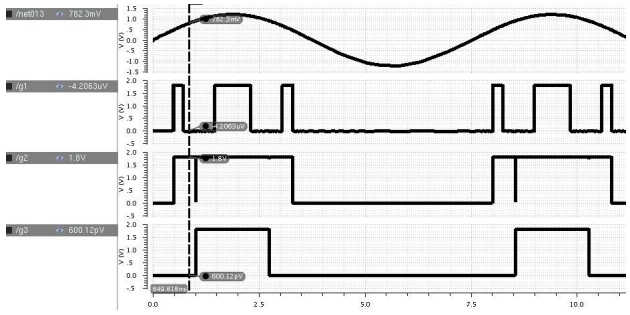

Fig.12.Waveform for ADC

The requirement of Hardware for Flash ADC doubles for a resolution with increase in one bit which makes it suitable for low resolution. The Power dissipation increases by a

factor of two as the requirement of comparator scales in response to resolution. In response, the CPL logic compensates for the power to some extent in this Flash ADC.

2.2. Design for Test (DFT):

There are possibly three ways for testing the high speed data converters. The most used method involves the down-sampling of the ADC output using on-chip de-multiplexer followed by a conventional Low Noise Amplifier for capturing the digital data for analysis purpose. Basically, the outputs that can be down sampled directly without filtering is expensive and hard to implement as an at-speed decimation filter on chip by complicating the hardware requirement. As a result, the measured noise floor keeps on increasing as the high frequency noise is folded behind the baseband of the down sampled spectrum. The alternative method is by implementing the superfast on-chip memory to store the ADC‘s output. Similarly, the hardware cost is expensive and the design is complicated. The simplest method is to use a digital loop-back technique[10]. This method requires the simplest and the least on-chip circuits and thus well suited test circuit which is depicted as in Fig.13.

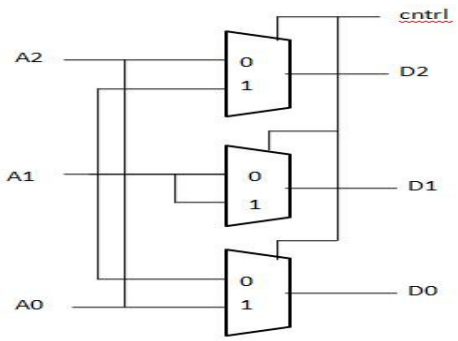

Fig.13.Circuit for DFT

The Design for Test block enables the test chip to conduct the at-speed tests in the cascaded mode, or to perform the eye diagram tests in the shuffled mode [16]. A control pin Ctrl that is shown in Fig.11 is used to switch between the cascaded mode and shuffled mode.

In the Cascaded mode ,the given Ctrl input is 0.In this mode, the digital outputs of ADC are directly connected to the corresponding inputs of the DAC. That is, the DFT design makes use of digital loop-back technique for addressing the at-speed testing issues. The differential nonlinearity (DNL) and integral nonlinearity (INL) values are measured by periodically applying a sine input to the ADC in this cascaded mode. Then, the output waveform of the DAC is obtained by plotting the transfer curve of the ADC‘s input and the DAC‘s output. The transition voltages in this staircase plot can be used to derive the DNL and INL of the ADC, while the analog output levels of the DAC can be used for computing the DNL and INL values of the DAC. In the shuffle mode, the given Ctrl input is 1. In this shuffle mode, the DFT circuitry shuffles the connection order of the digital loop-back such that the LSB of the ADC *A*0 connects to the MSB of the DAC *D*2, *A*1 to *D*1, and so forth.

As the LSB of the ADC‘s output is the most random bit and the MSB is the least random bit, the shuffled codes become a randomized digital signal which makes it suitable for the eye-diagram tests. The combined output of DFT and DAC is shown in Fig.14.

2.3. DAC:

Digital to Analog Converter is used to convert digital quantity into analog quantity.DAC Converter produces an output current of voltage proportional to digital quantity applied to its input. Today microcomputers are widely used in industrial control. The output of the microcomputer is a digital quantity. In many applications the digital output of the microcomputer has to be converted into analog quantity which is used for the control of relay, small motor, actuator etc., In communication system digital transmission is faster and convenient but the digital signals have to be converted back to analog signals at the receiving terminal.DAC Converters are used as a part of the circuitry of several Data Converter Pairs [6]-[9] and .

Gray coding representation is used in all global applications. The output from the ADC followed by Design for Test Circuit will also be a Gray Code. In Gray coding, the adjacent representations (symbols) differ by only one bit. Gray coding, when combined with Forward Error Correction codes capable of corrective single bit errors, it can aid in correction of erroneous reception of bits that spills into adjacent symbols. Digital modulation techniques like M-PSK and M-QAM use Gray coding representation to represent the symbols that are modulated. In M-PSK and M-QAM modulation techniques if the constellation symbols are Gray encoded, and then the adjacent constellation symbol differs only by one bit. Thus this Gray encoded structure gives a lesser probability of error than natural binary ordering. Gray code is useful because only one bit changes at a time. When used as encoders for a position sensor, for instance, if the sensor were right at the edge of a change boundary, there is uncertainty. This is the reason why Gray coding is preferred in all real time applications involving ADC.

Hence the Gray to Thermometer Decoder acts as a DAC in this Data Converter Pair. The combined output of DFT and DAC is shown in Fig.14.

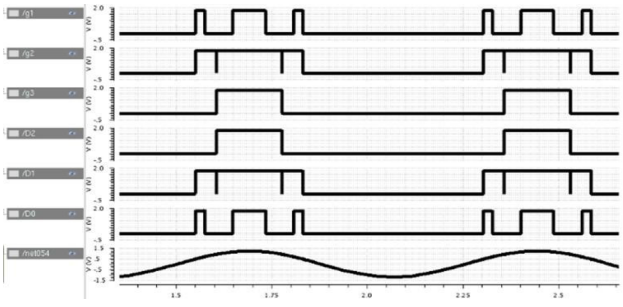

Fig.14.Output of combined DFT and DAC

III CONCLUSION

Thus, the Data Converter pair that is comprised of Analog to Digital Converter, DFT and Digital to Analog Converter is designed using Cadence 180nm technology.The INL error for the ADC is within −0.45 to 0.45 LSB respectively. The use of CPL Logic allows the reduction in power consumption consuming 620 mW and 110 mW for ADC and DAC from a 1.8-V supply, respectively.The future work involves the further reduction in power by using advanced logic such as Domino Logic for the replacement with CPL logic.

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