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Decoder Design Using Gate Diffusion Input Technique

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***Abstract*— In the modern age, there is an immense need of applications which consume less power and are small in area. In this paper, an effort is made to come up with one such application called the 2-to-4 line decoder using the AND gate. Some logic styles like CMOS, TG, PTL and GDI are used for the comparison analysis. It is observed that the GDI technique consumes both less power and area when compared to CMOS, TG and PTL logics. The proposed GDI 2-to-4 line decoder is designed and simulated using DSCH 3.1 and Microwind 3.1 on 32nm. The proposed circuit comprises of 10 NMOS and 10 PMOS. Power comparison analysis is done on MOS model called the Empirical Level-3. The analysis show that the area consumed by the proposed circuit is 19.76 µm^2 at 0.35V power supply and consumes 0.014µW power . Therefore, after comparison with the other three logics i.e. CMOS, TG and PTL it is found that the proposed circuit proves to be more area and power efficient.**

***Index Terms*— 2-to-4 line decoder, CMOS, Transmission Gate, Pass Transistor logic, Gate Diffusion Input, DSCH, BSIM**

I. INTRODUCTION

In the present world of technology, the reduction in power is the major issue. In high performance digital systems, such as microprocessors, digital signal processor (DSPs) and other applications, the low power designs are of great importance. In this paper an attempt is made to achieve a power and area efficient 2-to-4 line decoder using the GDI technique. Decoders are basically combinational circuits, which convert n-bit information into a maximum of 2n output lines. They are used where, on the occurrence of specific combinations of input levels an output or a group of outputs are to be activated. These input levels are often provided by the outputs of a counter or register. When the decoder inputs come from a counter that is being continually pulsed, the decoder outputs will be activated sequentially, and they can be used as timing or sequencing the signals to turn devices ON or OFF at specific times. A wide use of decoders is made in the memory systems of computers. In the memory systems the decoders, respond to the address code input from the central processor to turn on the memory storage location specified by the address code[1].

A. DECODER

A Decoder is a combinational circuit that converts an n-bit binary information into 2n output lines such that only one output line is activated for each one of the possible combinations of inputs. The n inputs are a combination of 0's and 1's. For each of the input combinations only one of the outputs will be active (HIGH), while all other outputs will remain inactive (LOW).[2]

In this paper, a 2-to-4 line decoder is proposed which is implemented using four logic styles called the CMOS, TG, PTL and GDI. All these logic styles make use of AND and NOT gates to implement the 2-to-4 line decoder. The two inputs to the proposed decoder are A and B, whereas D0 through D3 are the four outputs. CMOS devices nowadays are a part of the existing VLSI technology because of its special characteristics like the negligible standby power, due to which tens of millions of transistors can be incorporated on a single processor chip. There are certain drawbacks of the CMOS devices among which the ones of our concern with respect to this paper are: the use of large number of PMOS transistors, which result in high input loads[8], and secondly when the channel length is reduced to the nanometer level, because of thermal injection and quantum-mechanical tunneling the electrical barriers in the device begin to lose their insulating properties. As a result there is a fast increase in the standby power of the chip, thereby putting a limit on the integration level in addition to the switching speed[3]. The general block diagram of 2-to-4 line decoder is shown in figure 2.The boolean expressions for the output of the 2-to-4 line decoder are as follows

$$D_0 = \overline{A}\,\overline{B} \quad (1)$$

$$D_1 = \overline{A}B \quad (2)$$

$$D_2 = A\overline{B} \quad (3)$$

$$D_3 = AB \quad (4)$$

The equation below represents the consumption of power of a CMOS digital circuit:

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$$P = fCVdd^2 + fI_{short}Vdd + I_{leak}Vdd \quad (5)$$

Here f is the clock frequency, C is the average switched capacitance per clock cycle, VDD is the supply voltage, Ishort is the short circuit current, and Ileak is the off current[7]. The stand-by power consumption is represented by the 3rd term. An efficient way to reduce the dynamic power consumption is by means of a lower value of Vdd, since the 1st term is proportional to the square of Vdd. It is also to be noted that the short circuit and leakage power dissipation are also strongly dependent on Vdd. The lower the supply voltage, smaller is the power consumption. However, using a lower Vdd degrades the performance[6]. Two basic approaches to reduce power consumption of circuits in scaled technologies are: reducing the dynamic power consumption during the active mode operation of the device and the reduction of leakage current during the stand-by mode [8] . The simple combination of two complementary transistors is called a transmission gate or a pass gate. Due to the simplicity and low propagation delay of the transmission gates they are often used internally in the larger scale CMOS devices[6] The GDI logic style allows the implementation of a vast range of complex functions using minimum number of transistors. This is a suitable logic style for design of low-power circuits, since a reduced number of transistors are used in comparison to CMOS, PTL and TG logic styles. Simultaneously static power characteristics and logic level swing are improved thus allowing top-down design by using small cell library[7].

B. AND MODULE

The literature shows the different AND gates implemented by the different logic styles. Since AND is the major building block of the 2-to-4 line decoder, thus by reducing the number of transistors in the AND gate the area and power can also be simultaneously reduced.

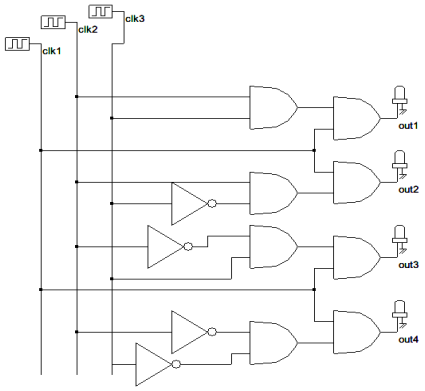

Figure 3: CMOS AND Design[6]

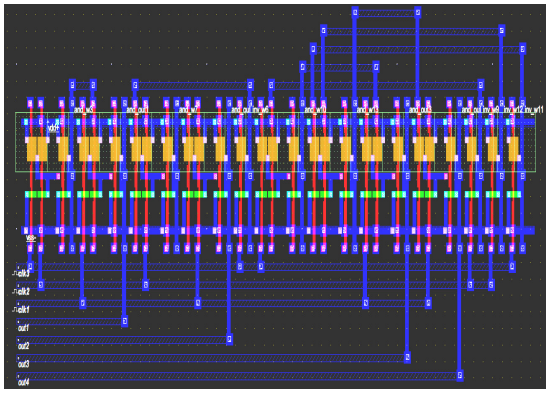

Figure 4: Layout design of CMOS AND design

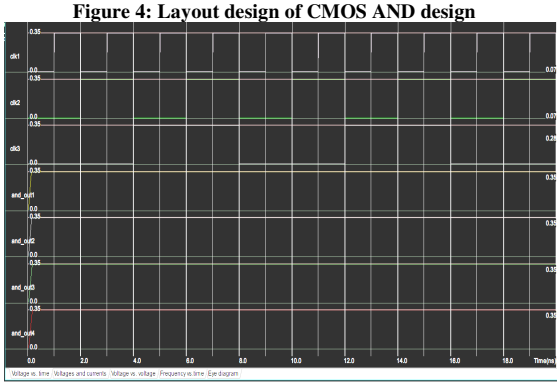

Figure 5: Simulation output of CMOS AND design

Figure 3[6] and Figure 4[6] shows the CMOS and TG AND designs. It can be seen that this CMOS design comprises of 6 transistors whereas the TG Design comprises of 5 transistors. Although both these designs provide a complete voltage swing between 0 to Vdd but at the same time they have a drawback of having large areas and also consume more power.

II. PREVIOUS WORK

In the past the 2-to-4 line decoder was implemented by using the Cadence designer tool. Figure 7[5] shows a 2-to-4 line decoder, it shows the simulation of decoder with the help of PMOS and NMOS transistor based on 45 nm technology. Transistors were operated on 0.7 V. The layout of the 2-to-4 decoder is also reduced with the help of 45 nm technology. So by using the 45 nm technology in the place of 180 nm technology the chip area , power consumption and leakage current can be reduced[6,7]. The reduction of leakage current and power is shown in this paper with the help of simulation tool. 2 to 4 decoder is simulated with the help of AND and NOT gates as shown in the F

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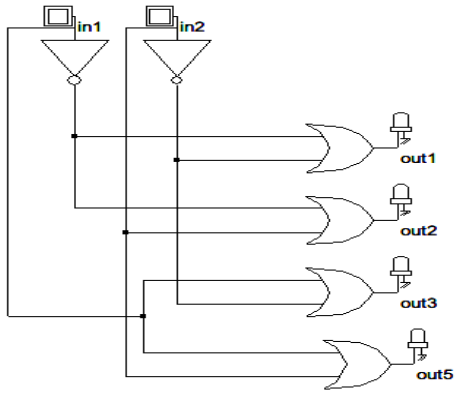

Figure 6: CMOS OR design Schematic diagram of 2 to 4 line decoder

In digital systems decoders play a vital role. Basically decoders interpret the input address to select a single data bit. It is a circuit which changes a code into a set of signals. It is known as a decoder because it igure 1. [8] performs the reverse operations of encoding. Decoders are simply a group of logic gates which are set in a specific way so as to breakdown any combination of inputs to a set of terms that are all set to '0' apart from one term. Therefore when one input changes, two output terms will change. A 2-to-4 line decoder makes use of two inputs namely A and B and four outputs, D0 through D3. Figure 8 illustrates a 2-to-4 line decoder. It is observed from the figure that all the outputs of the decoder are the AND combination of the two bitsThe proposed decoder of figure 9 is implemented using 4 GDI AND modules. The decoder comprises of 2T AND module The D3 output is the product of inputs A and B, D2 output is the product of input A and Inverse of input B. Similarly the outputs D1 and D0 are the products of input B and inverse of input A, and Inverse of inputs A and B respectively. Figure 10 shows the timing diagram of GDI 2-to-4 decoder. Before the actual layout design of GDI 2-to-4 decoder, it is necessary to authorize the schematic of the logic circuit. For this purpose the DSCH and MICROWIND designing tools work parallely. Design is first simulated on DSCH designing tool to know the exact working of the circuit and it is then implemented on the layout in MICROWIND

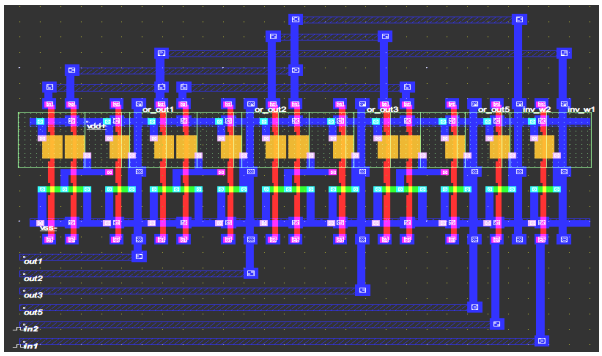

Figure 7: Layout design of CMOS OR design

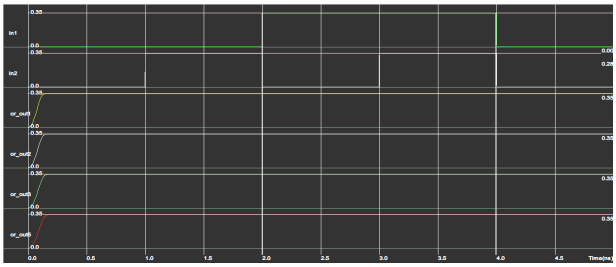

Figure 8: Simulation output of of CMOS OR design

III. PROPOSED DECODER DESIGN

The manual layout designing of a intricate circuit becomes very difficult. Thus in comparison to the manual layout designing it is preferred to use an automatic layout generation approach. In this paper DSCH designing tool is used to first design the schematic diagram at logic level. While DSCH 3.1 has the feature to examine timing simulation as well as power consumption at logic level but still the accurate layout information is missing. The VERILOG file is generated using DSCH 3.1 tool which is then compiled by the MICROWIND to create the corresponding layout with desired design rules. A different way to construct the design is by NMOS and PMOS devices using cell generator provided by the MICROWIND 3.1. This technique avoids any design rule error. The MOS generator option on MICROWIND tool can be used to adjust the length and width of the circuit.

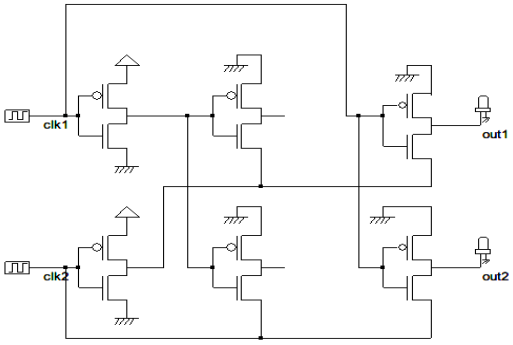

Figure 9:Proposed GDI 2 to 4 Decoder

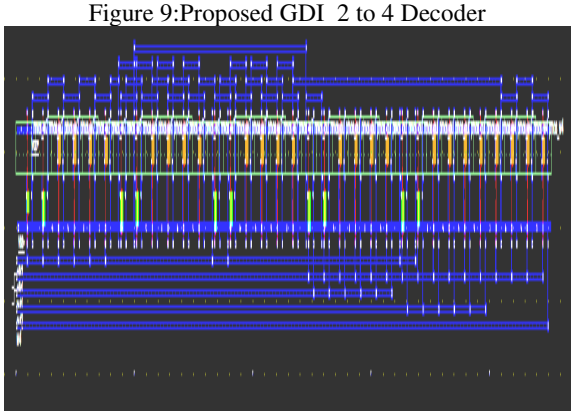

Figure 10: Layout design of Proposed GDI 2 to 4 Decoder

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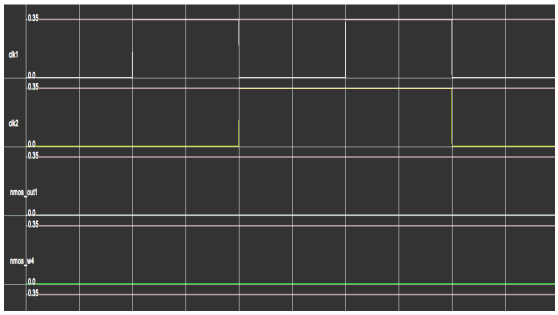

Figure 11: Simulation output of GDI 2 to 4 decoder

IV. SIMULATION RESULTS

To ensure the performance of proposed 2-to-4 line decoder design 32nm technology has been used. The evaluation is done in terms of area and power. MICROWIND 3.1 has been used for the simulation purpose. All results have been measured on MOS Empirical model Level-3 at on operating voltage 0.35V and operating temperature has been taken as 270C.

Table 1: Performance comparison of different decoders

	Power µW	area µm²	Memory in %	PMOS devices	NMOS devices	Electrical nodes
2 to 4 decoder with AND gates	0.172	49.6	6.3	28	28	50
2 to 4 decoder with OR gates	0.239	24.4	2.7	14	14	29
GDI 2 to 4 decoder	0.014	19.76	2.2	10	10	25

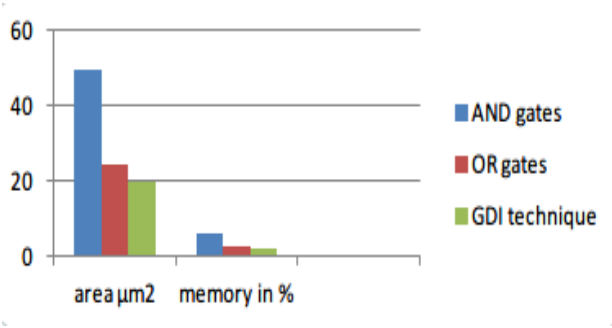

Figure 12 : Area & memory compression of different decoder circuits

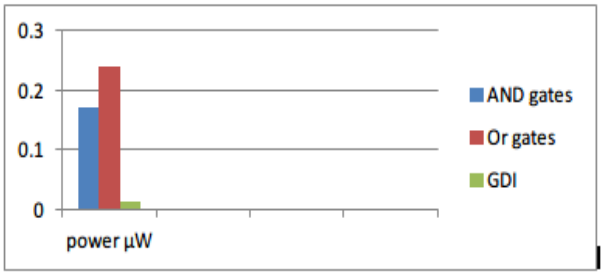

Figure 13: Power dissipation compression of different decoder circuits

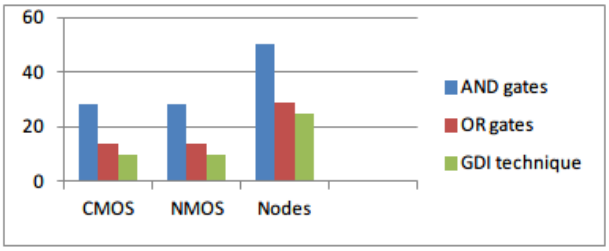

Figure 14: NMOS devices ,PMOS devices and electrical node compression of different decoder circuits

V. CONCLUSION

An alternative 2-to-4 line decoder by GDI approach has been proposed which comprises of only 20 transistors. The proposed 2-to-4 line decoder design has been implemented by using 10 NMOS and 10 PMOS transistors. The proposed design has been designed using an area and power efficient AND module which has been further implemented by using only 2 transistors. This area efficient GDI AND module has been used in proposed 2-to-4 line decoder design. The area and power simulation of proposed design has beendone using 120nm technology. LEVEL-3 and BSIM-4 models are used to depict the simulation results. Results show that on 32nm technology the area consumed by the proposed 2-to-4 line decoder GDI design is 19.76µm^2 .At 0.35V input supply voltage the proposed GDI 2-to-4 line decoder design consumes 0.014 µW power at LEVEL-3 . The proposed design can work efficiently with minimum supply voltage of 0.35V and can work on wide range of frequency between 2MHz to 400MHz. Simulation results of the proposed design show that the power consumption is less than rest of the models.

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