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AN EFFICIENT ARCHITECTURE WITH OPTIMIZED XOR DESIGN

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Abstract-The rapid growth of portable electronic devices, it is becoming a critical challenge to design low-power, high-speed (LPHS) circuits that occupy small chip areas. The dedicated short-range communication (DSRC) standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. In this project, the similarity-oriented logic simplification (SOLS) technique is proposed to design encoding circuits. We also propose XOR/XNOR circuits as the most significant blocks of digital systems with a new systematic cell design methodology (SCDM) in hybrid-CMOS logic style. This project not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

I INTRODUCTION

In 1999, the U.S. Federal Communication Commission allocated 75 MHz of Dedicated Short- Range Communication (DSRC) spectrum at 5.9 GHz to be used exclusively for vehicle-to-vehicle and infrastructure-to vehicle communications. The primary purpose is to enable public safety applications that save lives and improve traffic flow. Private services are also permitted in order to lower cost and to encourage DSRC development and adoption.

The DSRC spectrum is divided into seven 10 MHz wide channels. Channel 178 is the control channel, which is generally restricted to safety communications only. The two channels at the edges of the spectrum are reserved for future advanced accident avoidance applications and high-powered public safety usages. The rest are service channels and are available for both safety and non-safety usage.

The modulation methods incorporate amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zero mean for robustness issue, and this is also referred to as dc-balance. The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance. The purposes of FM0 and Manchester codes can provide the transmitted signal with dc balance. Both FM0 and Manchester codes

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are widely adopted in encoding for downlink.

CMOS wideband switches are designed primarily to meet the requirements of devices transmitting at ISM (industrial, scientific, and medical) band frequencies. The low insertion loss, the high isolation between ports, the low distortion and the low current consumption of these devices make them an excellent solution for many high frequency applications that require low power consumption and the ability to handle transmitted power up to 16 dBm, like car radios, antenna switching, wireless metering, high speed filtering and data routing, home networking, power amplifiers and PLL switching [6]. To improve their bandwidth, wideband switches use only N channel MOSFETs in the signal path. An NMOS only switch has almost twice the bandwidth performance of a standard switch with NMOS and PMOS FETs in parallel. This is a result of the smaller switch size and greatly reduced parasitic capacitance due to removal of the P-channel MOSFET. N channel MOSFETs act essentially as voltage controlled resistors. The switches operate as follows:

Vgs > Vt -> Switch ON
Vgs < Vt -> Switch OFF

where Vgs is the gate-to-source voltage and Vt is defined as the threshold voltage above which a conducting channel is formed between the source and drain terminals.

Therefore, a well-organized design methodology can be regarded as a strong solution for the challenge. It is not try-and error-driven, which means that it systematically and deliberately aims to the design goals. It also picks circuit components wisely and does not postpone the determination of the circuit characteristics after simulation. Cell design methodology (CDM) has been presented to design some limited functions, such as two input XOR/XNOR and carry–inverse carry in the hybrid-CMOS style.

Therefore, after the systematic generation, we proposes the SCDM considers circuit optimization based on our target in three steps: 1) wise selection of the basic cell; 2) wise selection of the amend mechanisms; and 3) transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. We consider the power-delay product (PDP) as the design target. It stands as a fair performance metric, precisely involving portable electronic system targets. The motivation to use this methodology is the presence of some unique features and the ability to produce some efficient circuits that enjoy all these advantages.

The rest of this brief introduces the concept based on VLSI encoding schemes and the switching activities for power consumption have discussed in section I and the related works and FM0/Manchester encoding using SOLS techniques are presented in Section II. Then, in Section III, the proposed

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methodology is presented. Section IV presents a experimental Results and Section V presents a performance analysis to illustrate the effectiveness of the approach. Finally, the conclusions are summarized in Section VI.

II RELATED WORKS AND FM0/MANCHESTER ENCODING USING SOLS

Here the VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications. The dedicated short-range communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. The similarity oriented logic simplification (SOLS) technique is proposed to overcome this limitation. The SOLS technique improves the hardware utilization rate for both FM0 and Manchester encodings. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

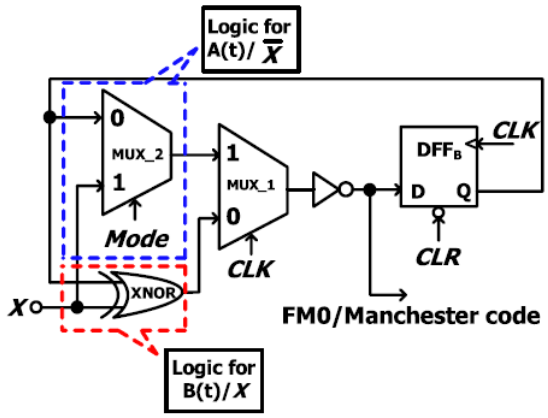

Fig.1: Balance computation for VLSI architecture of FM0 and Manchester encodings using SOLS technique.

The unbalance computation time between *A(t)/X* and *B(t)/X* results in the glitch to MUX−1, possibly causing the logic-fault on coding. To alleviate this unbalance computation time, the architecture of the balance computation time between *A(t)/X* and *B(t)/X* is shown in Figure. The XOR in the logic for *B(t)/X* is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for *A(t)/X*. This shared inverter is relocated backward to the output of MUX−1. Thus, the logic computation time between *A(t)/X* and *B(t)/X* is more balance to each other. The adoption of FM0 or Manchester code depends on Mode and CLR. In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware

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initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller. Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved.

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components.

III PROPOSED METHODOLOGY

In this section, the methodology for three input XOR/XNORs is presented according to the flowchart shown in Fig. 1(a). The design path is started by EBC systematic generation. In this step, general design goals are considered that the most distinctive ones are generating fairly balanced outputs, symmetric and power-ground-free structure, less transistors in the critical path, as well as sharing common sub-circuit. Systematic generation process of EBC in details is discussed in Section III-A. In the remaining steps, the methodology offers opportunity to strive toward an assigned design target. Two of these steps include wisely selection of mechanisms and basic cells from PDP point of view. An in-depth analysis for the selection in terms of PDP is presented in Section III-B. In the last step, in order to put the resultant circuits in proper state, a sizing algorithm consistent with the methodology is indispensable. In this line, SEA algorithm that is simple exact algorithm with the capability of determining goal is picked [17].

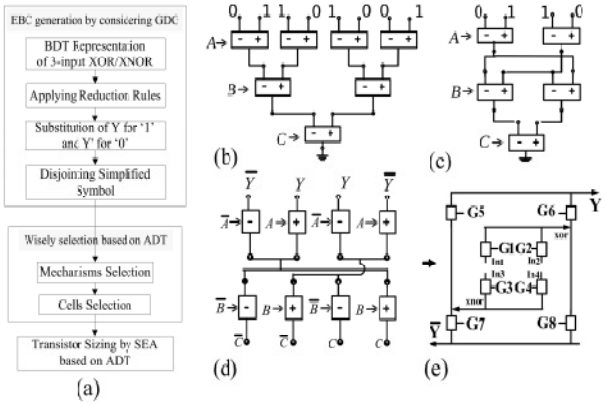

Figure 2: (a) SCDM process for designing efficient three-input XOR/XNORs. (b) BDT representation of three-input XOR/XNOR function. (c) Applying reduction rules. (d) Substitution and disjointing. (e) EBC.

The motivation to use this methodology is the presence of some unique features and the ability to produce some efficient circuits that enjoy all these advantages.

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1) The SCDM divides a circuit structure into a main structure and optimization-correction mechanisms. In the main structure, it considers features including the least number of transistors in critical path, fairly balanced outputs, being power ground- free, and symmetry. The mechanisms have the duty of completing the functionality of the circuits, avoiding any degradation on the output voltage, and increasing the driving capability.

2) The least number of transistors in critical path increases the chances of the circuit to have better characteristics in terms of delay and Energy-Delay Product (EDP), respectively.

3) The dynamic consumption optimization comes from the fact of well-balanced propagation delay. This feature is advantageous for applications in which the skew between arriving signals is critical for proper operation, and for cascaded applications to reduce the chance of making glitches [2].

4) Power-ground-free main structure leads to power reduction.

5) Symmetrical structure, high modularity, and regular arrangement of designs give rise to sharing more wells of connected transistors and in turn reducing the occupied area .

6) The degradation in all output voltage swing can thus be completely removed, which makes the design sustainable in low *V*DD operations and low static power dissipation.

7) Internal logic structure of designs has the potential to be energy efficient due to the combined reduction of power consumption and propagation delay.

8) SCDM utilizes the benefits of different logic styles as the hybrid style [2].

9) The methodology has high flexibility in target and systematically consider it in the three design steps. This can lead to efficient circuits in terms of performance, power, PDP, EDP, area, or a combination of them.

10) The fast evolution of microelectronics fabrication processes demands a new cell library generation or a library technology migration. The well-organized systematic methodology leads to automated flow, which can reduce design time and costs, provide consistency in the cell library generation process, increase the range of simulation capabilities at the characteristics step, as well as minimize the risk of errors [11], [12].

IV EXPERIMENTAL RESULTS

The proposed has been simulated and the synthesis report can be obtained by using Xilinx ISE 12.1 and the schematic result of proposed SCDM has been developed by TINA(fig.4). The various parameters used for computing existing and proposed systems with Spartan-3 processor are given in the table1 and also the waveform for the proposed shown in fig.3

s.no	Parameter	Existing(cmos)	Proposed (SDM)
1	Number of	12	8

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	transistor		

Table 1: comparison table for existing and proposed

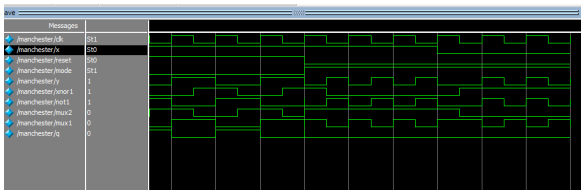

Fig3: simulation result for fm0/manchestor

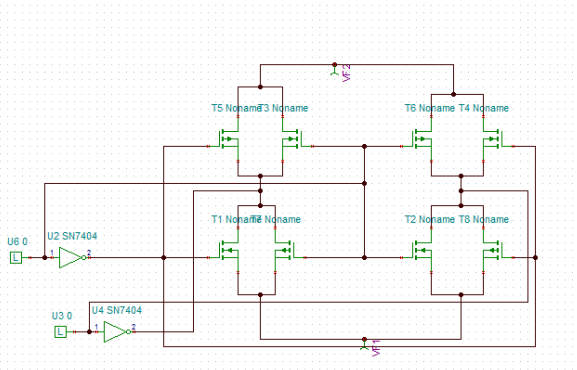

Fig.4 Schematic result of Proposed XOR/XNORs

V PERFORMANCE ANALYSIS

The Figure given below is shown that there is a considerable reduction based on no of transistors and the performance chart has been shown below in fig.5

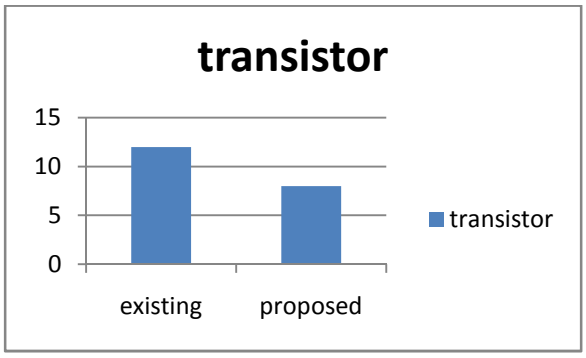

Fig.5 performance measure of existing and proposed

V CONCLUSION

In this project, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques. area compact retiming and balance logic-operation sharing. We also introduce new systematic cell design methodology (SCDM) in hybrid-CMOS logic style to design a xor gate in sol architecture .it provides high flexibility in design target, while it follows the same procedure to obtain the state-of-the-art designs. This project not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works.

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