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Fast and Reliable SDR Based Flight Termination System Analysis and FPGA Implementation Using OFDM

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Abstract— **This paper proposes a SDR based flight termination system analysis and FPGA implementation using OFDM. This is a new kind of FPGA implementation of digital FTS in SDR platform. This kind of implementation replaces a multiple platform with a single platform. The FPGA implementation based on FTS provide efficient optimization technique, very fast and very high reliable with ruggedized platform. In order to minimize hardware resources and to enable future up-gradation for efficient optimization technique. It also guarantees reconfigurable, interoperable, portable and handy FTS and maintains errorless, bug free and reliable implementation. Hence, XILINX and Model-SIM are used to simulate and implement the system in real-time and enables rapid prototyping. And it also provides automatically error detection and correction will be done over the SDR based communication system between the transmitter and receiver on FTS. Further the intermediate stages of processing were validated as an integrated system at real-time telecommunication operation environment.**

***Index Terms*— Field-programmable gate array (FPGA), flight termination system (FTS), real-time system, software defined radio (SDR), Orthogonal frequency-division multiplexing (OFDM)**

I. INTRODUCTION

A newly developed, Flight Vehicle (FV) needs rigorous testing to satisfy all expected performance. When testing the FV dynamically, there are lots of uncertainties regarding the flight performance. Hence at test facility, a flight termination system (FTS) is utilized to secure the property and human life. FTS basically involves in generation and transmission of remote command signals to the airborne flight vehicle to execute some operation inside the vehicle as required.

FTS is used for termination of high speed FV under test. Termination of test vehicle is mandatory if the high speed vehicle deviates from its preset trajectory and takes different course due to unpredictable failures of onboard system. In such cases specific commands are transmitted from command transmission system (CTS) for termination of test vehicle via remote control unit (RCU). The commands are transmitted when required during test. Real-time flight termination operation demands a very highly reliable and ruggedized platform. The commands transmitted by CTS is received and decoded by onboard command reception system (CRS) at FV and the commanded operation is done accordingly.

The design of FTS involves real-time signal generation, transmission and analysis of the transmitted signal. The system also has to ensure real-time communication with RCU with various demanded protocols. The system versatility with respect to different modulation schemes must be ensured for future up-gradation.

A suitable software defined radio (SDR) platform has proven itself to be very efficient platform for implementing such versatile and reconfigurable system architecture. SDR in recent trend is a common term, which has been used for rapid prototyping of different types of complex communication system used in different fields, such as for radar design , GPS receiver design, adaptive optics system design , drive servo system design etc. Many real-time applications such as advanced control system design, system performance measurement, data acquisition and processing use the FPGA integrated with PXI platform for implementation.

High robustness and high reliable flight termination operations are strongly desired. High degree of versatility and reconfigurable architecture with real-time response is achievable through the combination of highly reliable software with wide range of capabilities and suitable hardware platform i.e. FPGA. It is necessary to have system which is flexible, reconfigurable and dynamic to the environmental situations and hardware modifications. SDR based on FPGA system could be a good option for designing intelligent and reconfigurable CTS for operations on a single platform, as compared to the previously used bulky CTS, which was a discrete component based fixed configuration system. Different hardware based CTS systems were used for test of different flight vehicles. The newly developed SDR

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based FTS system in turn, solves the problem of frequent hardware replacements and cost of design as in SDR based system, only software updating is required to implement new system.

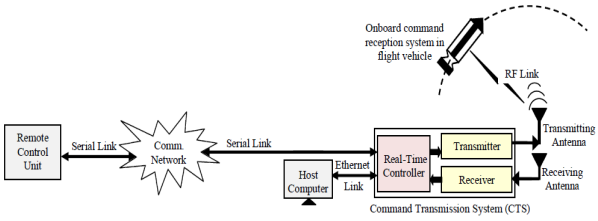

Fig. 1. The block diagram of the FTS transmitting signal to flight vehicle

The FPGAs are broadly used now-a-days for many applications. Because of efficient computational power, parallel data processing, low power consumption and technologies include as many as dedicated digital signal processor (DSP) cores to fit several order complex algorithms to be implemented. Further it is necessary to optimize the design algorithms for optimal resource utilization.

The FTS algorithm has been implemented in FPGA, which is optimized for DSP and memory intensive applications with low power serial connectivity. Model-SIM and Xilinx FPGA module has been used to simulate and design the various modules of the system. These Modules enables to simulate various modules of the system in faster way and the advantage is that the same simulation applies in real hardware implementation. The design has been implemented using fixed point data type, so as to optimize the resource utilization within the FPGA.

The CTS system consists of a real-time controller (RTC), host computer and SDR based command transmission and reception unit. The RTC offers a communication interface between RCU and host computer with CTS system. RCU is used for remote operation of the CTS. Host computer is used for configuration, local mode operation and analysis of intermediate signal processing of the CTS system.

A. *OFDM*

Orthogonal frequency-division multiplexing (OFDM) is a method of encoding digital data on multiple carrier frequencies. OFDM has developed into a popular scheme for wideband digital communication, used in applications such as digital television and audio broadcasting, DSL Internet access, wireless networks, power line networks, and 4G mobile communications.

OFDM is a frequency-division multiplexing (FDM) scheme used as a digital multi-carrier modulation method. A large number of closely spaced orthogonal sub-carrier signals are used to carry data on several parallel data streams or channels. Each sub-carrier is modulated with a conventional modulation scheme at a low symbol rate, maintaining total data rates similar to conventional single-carrier modulation schemes in the same bandwidth.

The primary advantage of OFDM over single-carrier schemes is its ability to cope with severe channel conditions without complex equalization filters. Channel equalization is simplified because OFDM may be viewed as using many slowly modulated narrowband signals rather than one rapidly modulated wideband signal. The low symbol rate makes the use of a guard interval between symbols affordable, making it possible to eliminate inter symbol interference(ISI) and utilize echoes and time-spreading (on analogue TV these are visible as ghosting and blurring, respectively) to achieve a diversity gain, i.e. a signal-to-noise ratio improvement.

II. SDR BASED FTS ALGORITHM

A. *Mathematical Formulation*

The concept of FTS is depicted in Fig. 1. The RCU is connected with the CTS through reliable serial communication links. The commands are given from the RCU to CTS. The commands are generated and transmitted from the CTS, received by onboard CRS through RF link and required operation is done accordingly.

The generated commands are a frame of binary bits. This frame comprises of n number of binary data bits, which is headed by h number of binary header bits and trailed by s optimized area; FPGAs are presently taking over legacy processor based applications. Current development in FPGA number of stop bits. So the length of the frame is . The whole frame is N = (n + h + s) encoded with Manchester encoding scheme and total number of bits in a frame becomes double i.e.2N.

The frame is converted to binary data wave form with the logic d (t) = +1 or -1 corresponding to the binary bits 1or 0. Hence, the binary data waveform d(t) can be expressed as:.

$$d(t) = \sum_{i=0}^{2N-1} b_i \, P(t - i.T_b)$$

Here bi is the number of bit of the frame. The bit bi takes on value 1 and -1 for binary bit 1 and 0 respectively P(t) is a rectangular pulse which can be represented as P(t) = rect(t/Tb). Here, Tb is bit duration. This binary data waveform d(t) modulates a carrier signal using binary frequency shift keying (BFSK) modulation scheme. In this scheme sinusoidal signal with higher frequency and lower

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frequency are generated for bit 1 and 0 respectively. Thus, the BFSK modulated signal can be represented as:

$$BFSK(t) = A\cos\{\omega_0 t + d(t).\Omega.t\}$$

The carrier frequency Equation can be written as:

$$BFSK(t) = A\cos\left[\{\{\omega_0 + d(t)\}\Omega.t\}\right] = m(t)$$

This BFSK modulation is done in very low frequency i.e. in very low frequency band. This signal is finally up-converted to ultra high frequency band using FM modulation scheme. The basic principle behind FM is to vary the carrier frequency in proportion to the modulating signal m (t). This means instantaneous frequency of the carrier is changing in proportion to m (t). This can be written as,

$$\omega_i(t) = \omega_c + K_f.m(t) = \frac{d\theta(t)}{dt}$$

The generalized angle. Equation can be written as,

$$\theta(t) = \int_{-\infty}^{t}\{\omega_c + K_f.m(\alpha)\}\,d\alpha$$

Equation follows to,

$$\theta(t) = \omega_c t + K_f\int_{-\infty}^{t} m(\alpha)\,d\alpha$$

So the corresponding FM signal can be written as,

$$FM(t) = A_c\cos\left\{\omega_c t + K_f\int_{-\infty}^{t} m(\alpha)\,d\alpha\right\}$$

Here, At is amplitude of the career signal and modulating signal m (t) is BFSK modulated signal BFSK (t). In the receiving side, FM signal FM (t) can be demodulated by applying the signal to the differentiator. The output of the differentiator is,

$$F\dot{M}(t) = \frac{d}{dt}\left[A_c\cos\left\{\omega_c t + K_f\int_{-\infty}^{t} m(\alpha)\,d\alpha\right\}\right]$$

Equation follows to,

$$F\dot{M}(t) = A_c\{\omega_c + K_f.m(t)\}\sin\left\{\omega_c t + K_f\int_{-\infty}^{t} m(\alpha)\,d\alpha\right\}$$

This signal is both amplitude and frequency modulated. If for wc+kf.m (t)>0, for all t, m (t) can be recovered by envelope detection of FM (t) .Next step is to demodulate the BFSK signal for recovering the command frame. The BFSK signal is demodulated by a square law detection method.

B. SDR based design approach

For a conventional discrete component based design, it is not possible to vary the functionality of the system beyond certain range of specification. But a SDR based on FPGA enhances the capability of the platform so as to design a system with re-configurability and flexibility. The main philosophy behind SDR is that it can flexibly alter the radio waveforms by changing software and without changing the SDR platform. As in SDR, large part of the waveforms are defined in software, it allows us to flexibly change the waveforms within certain bounds by implementing the appropriate software modules.

SDR can be implemented in different platforms. A SDR based FTS including its main elements implemented in FPGA is depicted. The heart of the system is real-time operating system. The waveforms and their portability which includes the middleware are realized through basic functions and libraries provided by the software framework. The combination of software communication architecture and CORBA forms the software framework.

III. FPGA IMPLEMENTATION OF SDR BASED FTS

A. Realization of signal generation in Modelsim and Xilinx FPGA

In the presented application the SDR based telecommunication operation is realized in FPGA, using high level programming language. The command codes generation and encoding are done easily.

The essential problem during the implementation of SDR based telecommunication operation is realization of signal generation for modulation, digital up conversion (DUC), digital down conversion (DDC), demodulation, signal filtering etc. For this purpose, the signal is generated in Model-SIM FPGA using a technique called direct digital synthesis (DDS).

In DDS, a time varying signal is generated in digital form and then Digital to Analog Conversion is performed to obtain an analog waveform usually a sine wave.

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B. Code realization for FPGA

Optimization exists in the coding of FPGA and timing in various ways. In this project, the fixed point notation is used, which helps in achieving hardware resources utilization.

The Single Cycle Timed Loop is a special use of the timed loop structure enabling optimization of program. This loop executes all functions inside it within one tick of the FPGA clock in FPGA target. It can be used with derived clocks to operate the loop at a different rate and can be used with faster global clock (80 MHz or above). Use of shift register and feedback nodes in it enables us to implement parallel execution of logic and passing of data between subsequent iterations. The appropriate use of state machine for implementing different parts of the application in it provides speed and efficiency of the application.

The efficiency of the algorithm can be enhanced through appropriate use of pipelining technique. In this scheme, the algorithm is broken into smaller parts and those parts which can be executed independently are identified. Next, they are executed in parallel manner. The length of code executed in each iteration is reduced and the total time for implementing the whole application becomes less.

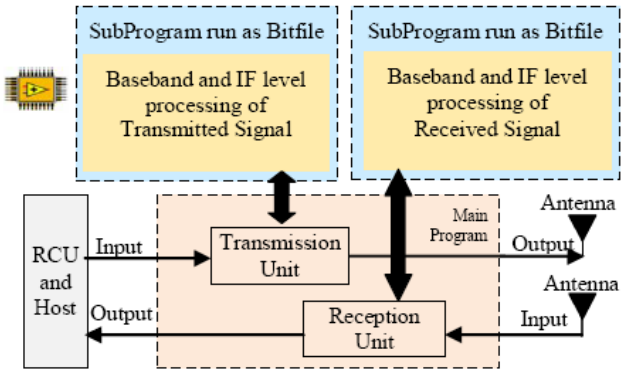

Fig..Board Software Implementation Scheme

During this implementation two very important factors considered are balancing of pipeline stages and minimization of memory transfer.

Effective compilation of the program in the target application may not be certain by applying these methods while realizing the SDR based FTS. For surmounting this problem a special program as depicted in, has been developed.

The algorithm comprises of two parts: the main program and the sub programs. The SDR based command transmission chain and command reception chain (CTS) are realized in the main part of the program.

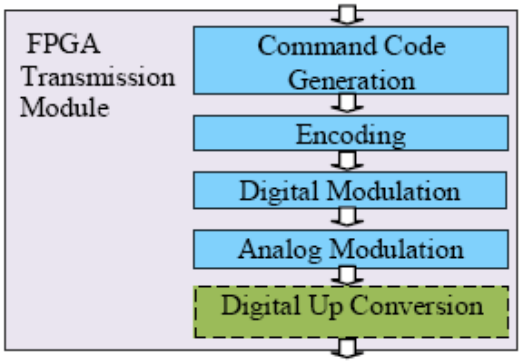

Fig. Transmission Module Implemented in FPGA

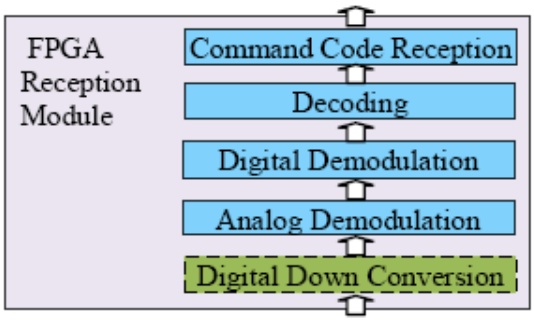

Fig. Reception Module Implemented in FPGA

The encoding (Manchester Encoding), decoding, modulation (FM modulation followed by BFSK modulation), de-modulation (Non coherent BFSK demodulation followed by FM demodulation), DUC and DDC are implemented in two FPGAs and are executed from the main program through bit file of respective program. Manchester encoding and decoding method is used and it includes error detection and correction method. Modulation, de-modulation, DUC and DDC are implemented as sub programs in FPGA VI, which allow the program to optimally use the logic elements.

During the data processing in each chain (Transmission chain and receiving chain), the main program transfers control to sub-programs, where output values are calculated simultaneously by the Sub VIs.

It should be noted that the application startup time of the system is very fast as the application is deployed in RTC. The change of any parameter setting can be done at real-time, which is very easy and fast as the data transfer between RTC and host occurs through TCP/IP and between RT and FPGA through FIFO and memory element.

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IV. EXPERIMENTAL SETUP

A. *Laboratory Setup*

The SDR based FTS includes FPGA, RTOS and GPUs. The communication algorithms, DDC and DUC are implemented in FPGAs. The analog to digital conversion, digital to analog conversion, RF up conversion and RF down conversions are implemented in high speed PXIe cards. The remote command interface is implemented in GPU connected to RTOS via reliable communication links. The SDR based FTS algorithms were implemented using high level programming language and were realized by NI PXI-7966R with Xilinx Virtex 5, SXT, and FPGA.

The experiment was done in 2 phases. Offline: The onboard receiver with decoder (nominal power of 12V DC) is kept in laboratory. Online: The onboard receiver with decoder is kept inside helicopter and received the status through ground telemetry stations.

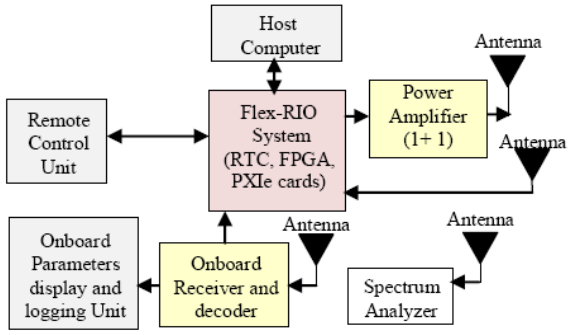

Fig: The block diagram of laboratory setup

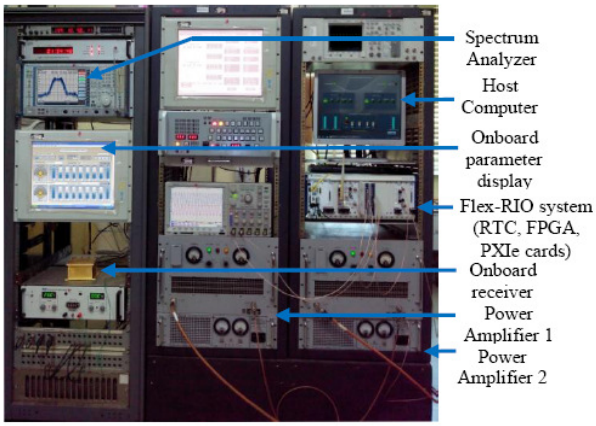

Fig: Laboratory Setup

The laboratory setup (Fig) is composed of one onboard receiver and decoder with receiving antenna. Initially different command codes and frequency of operation are set in the on board receiver. Then, the commands are transmitted from FTS with the same command codes and frequency set in onboard receiver. The delay between transmission and reception of command codes are observed and analyzed by taking feedback from the onboard decoder to the host computer.

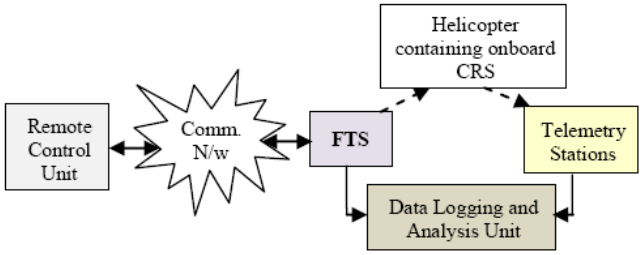

Fig. The block diagram of online setup

In online experimental setup, the onboard receiver with decoder is kept inside helicopter and received the status through ground telemetry stations and the same is fed to the host computer for analysis. In offline experimental setup, the onboard receiver with decoder is kept in laboratory and the received signal status information is fed to host computer through Ethernet link for analysis.

B. *Parameters Setting*

In both of the testing procedure, the commands are transmitted at different frequency band such as HF, VHF and UHF and the signal characteristics were analyzed. The system parameters setting were depicted in Table.

Table. SDR Based FTS Parameters setting

Parameters	Operation Range	Unit
Baseband Data rate	2-8	Kbps
BFSK Mark Frequency	0-50	kHz
BFSK Space Frequency	0-50	kHz
FM Deviation	100-200	kHz
IF Center Frequency	15-35	MHz
RF Up Conversion Center Frequency	25-2750	MHz
RF Down Conversion Center Frequency	25-2750	MHz

V. CONCLUSION

In this paper a SDR based FTS analysis is done on OFDM based transceiver. The system has been designed using Xilinx and Model-SIM tools. These tools are very flexible platform for complex algorithm for FTS system design. And its provides a very reliable and fast Error Detection and Correction methods are implemented on communication between the control unit and FTS transceiver system. Suitable algorithms for signal generation, encoding, baseband and pass band modulation, digital up conversion and down conversion, filter design have been chosen and implemented to ensure optimized uses of hardware. In future CDMA based FTS system can be implemented using developed SDR based

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framework for control of multiple flight object simultaneously.

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