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GLOBALLY SYNCHRONOUS AND ASYNCHRONOUS ROUTER FOR DYNAMIC VIRTUAL CHANNEL NOC SYSTEM

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ABSTRACT:

Most communication traffic in today's Network on Chip is originated on Router,synchronousmemoriesand I/O Channel. Channel should be designed to comfortably handle the many-to-one data exchange and access data using routing controllers the existing system uses adaptive synchronous and asynchronous router architecture to handle traffic efficiently andit justifies the power consumption and speed performance improvement with row hit rate.But DVC method is compatible for either synchronous or asynchronous NOC, rather latest processors fabricated as Multi core. More data entry time and failed to describe bottleneck conditions. So we used dynamic VC approach. It enhances data access and overcome synchronization errors when compared to traditional solutions. Globally Synchronous and Asynchronous (GSAS) based Network onChip optimizes memory and using thread row buffer. Our analysis takes place on a realistic NOC multimedia benchmark to prove large reduction in power consumption and improvement in performance and throughput compared to existing solutions.It raises data flow and performance of the NoC system. Globally Synchronous and Asynchronous Memory controller for Dynamic Virtual Channel-NOC to avoid bottleneck traffic and multiple end to-end data flow between NOC soft-core processors with high data rate and low area consumption and Row Hit Distributed Arithmetic (RHDA) method is comprised to reduce latency.

Key words—VLSI based Network on chip, priority Scheduling, GSAS Router.

I.INTRODUCTION

Network on chip is a communication subsystem on an integrated circuit generally called as chip, frequently between intellectual property (IP) cores in a system on a chip . It can amountsynchronous and asynchronous clock domains.conventional bus and crossbar intercon nections improves highly and it provide chip

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communication NoC improves the scalability of System on chip, and the power ability of complicated System in Chipcorrelated to other designs.In Efficient Dynamic Virtual Channel Mechanism, It utilizes the common features of Dynamically Allocated Memory Queues input port to generate a dynamic flow control. Virtual Channelis used discharged with the flit-data in the input-port buffer to supportthe Efficient Dynamic Virtual Channel mechanism in circulating the request signals to the moderator. Virtual Channel-full andVirtual Channel -block signals are needed to sustain the order of flits correlate with each Virtual Channel.The flit arrival time and departure time entirely associated to a parallel FIFO. There is no blockage, each incoming flit and its Virtual Channel -ID is gathered in the buffer station pointed by the write-pointer. The read-pointer is used to read data, moderatordepend on its Virtual Channel-ID and sent out of the buffer.

But it maintains additional delays and Hardware overhead due to recruit register updates and operations. DVC method is suitablefor either synchronous or asynchronous NOC, comparatively latest processors fabricated as Multi core. provide more data access time and failed characterizesbottleneck conditions It is used to process multi core functions and implement frequency synthesizer to hold multiple frequencies. To provide high speed data access between shared virtual memories a row hit protocol is introduced with DynamicVirtualChannel Priority based data access with RHP Reduces traffic congestion and hardware overhead it is Compatible for multi-core processors without area overhead. It maintains Tradeoff between speed and QOS.

II.Related Works

In [1] An effective end-to-end flow control scheme, called Hotspot prevention is used to resolve the hotspot congestion problem for the Close network on the chip Specifically, HOPE regulates the injected traffic rate proactively by estimating the number of packets inside the switch network destined for each destination and applying a simple stop and-go protocol to prevent hotspot traffic from jamming the internal links of the network

.In [4]An efficient NoC design is used which is based on the transaction protocols used by on-chip components.

In [5] A method for NoC topology generation and analysis is presented that incorporates on-chip communication behavior and attempts to generate minimal topologies, both in terms of resource usage aVirtual channels are quintessential constructs in the correct operation of both the NoC routing algorithm and the CMP's cache coherence protocol. It introduces the notion of VC Renaming, which enables the

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further virtualization of existing VC buffers, in order to decouple the number of supported VCs in the system from the number of physically present VC buffers.

In [8] a new approach for implementing virtual channels (VC) for multi-core interconnection networks is presented. Here the flits of different packets interleave in a channel with a single buffer of nominal depth by using a rotating flit-by-flit arbitration.

In[18]Two new virtual channel allocation (VA) mechanisms, termed Fixed VC Assignment with Dynamic VC Allocation (FVADA) and Adjustable VC Assignment with Dynamic VC Allocation (AVADA) is presented. The idea is that VCs are assigned based on the designated output port of a packet to reduce the Head-of-Line (HoL) blocking

In[19]Multi-VC dynamically shared buffer named DAMQ-PF for network on chip to decrease the memory and area requirement of statically allocating shared buffer among multiple virtual channels (VC).

III. PROPOSED SYSTEM

A. Globally Synchronous And Asynchronous (GSAS) architecture

A GSAS approach is introduced to process multi core functions and implement frequency synthesizer to support multiple frequencies. To make high speed data access between shared virtual memories a row hit protocol is introduced with DVC (Dynamic Virtual Channel). Globally asynchronous locally synchronous (GALS) is a Model of Computation (MoC) that emerged in the 1980s. It is based on synchronous programming and asynchronous programming.

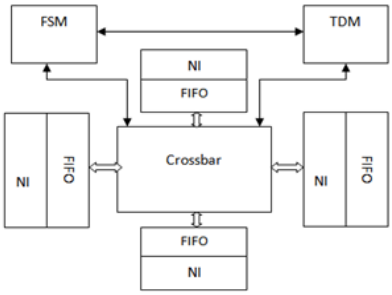

Fig1 Globally Synchronous and Asynchronous architecture

These changes are aggregated for synchronous circuit as most changes are initialized by an active clock edge. Therefore, large spikes on supply current A GALS circuit consist of a set of locally synchronous modules communicating with each other via asynchronous wrappers. Each synchronous subsystem ("clock domain") can run on its own independent clock (frequency). Advantages include much lower electromagnetic interference (EMI).

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The CMOS circuit (logic gates) requires relatively large supply current when changing occurs at active clock edges. These spikes can cause large electromagnetic interference, and may lead to circuit malfunction. In order to limit these spikes large number of decoupling capacitors are used. Another solution is to use a GALS design style, i.e. design (locally) is synchronous but globally asynchronous, i.e. there are different (e.g. phase shifted, rising and falling active edge) clock signal regimes thus supply current spikes do not aggregate at the same time. Consequently, GALS design style is often used in system-on-a-chip (SoC).

B. Priority based FIFO architecture

A priority queue is an abstract data type which is like a regular queue or stack data structure, but where additionally each element has a "priority" associated with it. In a priority queue, an element with high priority is served before an element with low priority. If two elements have the same priority, they are served according to their order in the queue. A priority queue is an abstract concept like "a list" or "a map"; just as a list can be implemented with a linked list or an array. priority queues typically O (log n) performance for inserts and removals, and O (n) to build initially. Variants of the basic heap data structure such as pairing heaps provide better bounds for some operation.

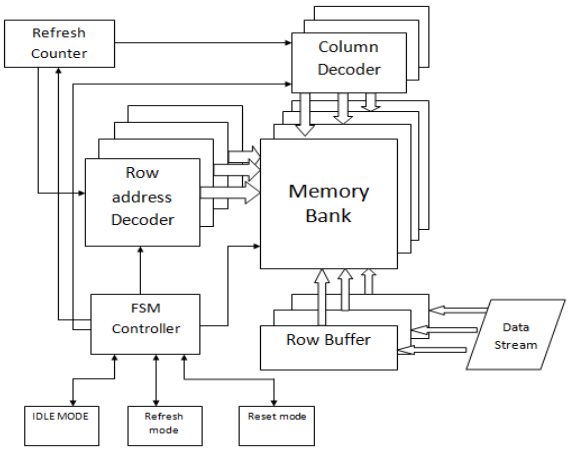

Fig2 priority based FIFO architecture

A priority queue must at least support the following operations:

insert with priority: add an element to the queue with an associated priority.pull highest Priority element: remove the element from the queue that has the highest priority, and return it

PERFORMANCE ANALYSIS:

Throughput:

It measures the total rate of data sent over the network, including the rate of data sent from source to router and data sent from node to destination

Congestion control:

In stack data Structure every element has a priority associated with it an element with high priority is served before an element with low priority hence it reduce traffic congestion

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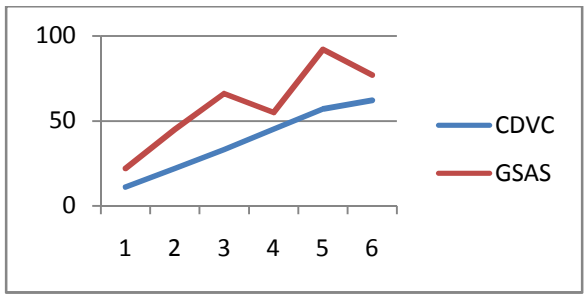
Delay:

The delay of a network specifies how long it takes for a bit of data to travel across the network from one node or endpoint to another. it is typically measured in multiples or fractions of seconds.

Overhead:

Overhead is any combination of excess or indirect computation, time, memory, bandwidth or other resources that are required to attain a particular goal



GSAS successfully brings out an improvement in latency by 45-50% and throughput by 70%.Time(s) is plotted along X axis and throughput is plotted along Y axis

IV. CONCLUSIO AND FUTURE WORK: - A Globally Synchronous and Asynchronous (GSAS) approach is introduced to process multi core functions and we implement frequency synthesizer to support multiple frequencies .To make high speed data access between shared virtual memories a Row Hit Distributed Arithmetic (RHDA) method is introduced with DVC (Dynamic Virtual Channel).where it is based on synchronous and asynchronous programming where is comprised to reduce latency. priority based data access with RHDA maintains tradeoff between speed and QOS .The proposed system reduces the hardware overheads and it become compatible for multi core processors without area overhead and finally it used all memory ports i.e. 100% efficiently

In future, re-organization of the existing single large row buffer in a DRAM bank into multiple smaller row-buffers. This configuration helps improve the row hit rates and also brings down the energy required for row-activations. The major contribution of this work is proposing such reorganization without requiring any significant changes to the existing widely accepted DRAM specifications.

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